Atari STe 520/1040
Computer Field Service Manual
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SECTION ONE:
INTRODUCTION

1.0 OVERVIEW

The 520STE and 1040STE are designed as integrated units with keyboard, processor, memory, and I/O control in one package. The 520STE has 520 kbytes (524,280 bytes) of RAM, and the 1040STE has 1040 kbytes (1,048,568 bytes) of RAM. The 1040STE and 520STE both have a built-in 1 megabyte floppy disk drive (unformatted). Both the 520STE and 1040STE come with a modulator for TV output. The 520STE and 1040STE both have the power supply integrated into the case.

1.1 MAIN COMPONENTS

- 524K RAM (1048K for the 1040STE)
- Main Board with modulator (except French Peritel)
- Keyboard Assembly
- RF Shield (upper and lower) and Power Supply
- Plastic Case (upper and lower)
- Mouse
- Power Supply
- Disk Drive

1.2 CASE DESIGN

The 520STE and the 1040STE are nearly identical. The upper case has openings for the keyboard and a lens for both the power indicator LED (front left corner) and the Disk Drive Activity LED (mid right side). **(see Fig. 1-1)**

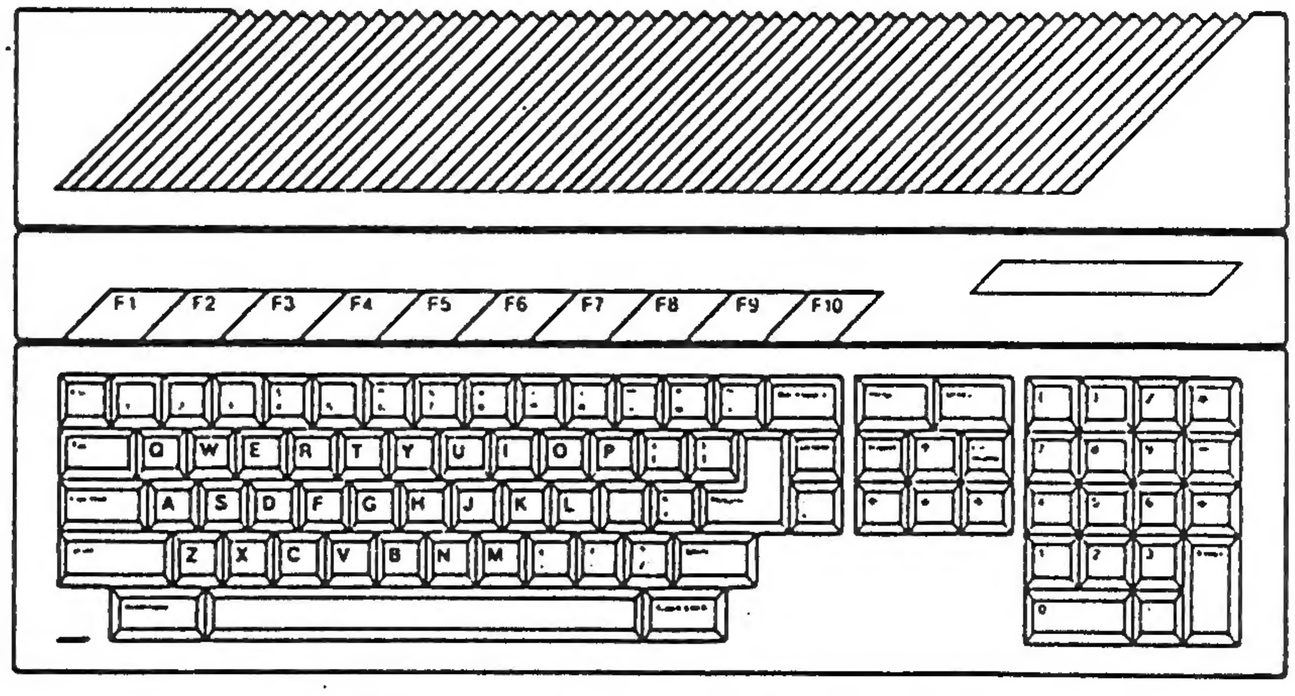


Figure 1-1: 520STE Upper Case

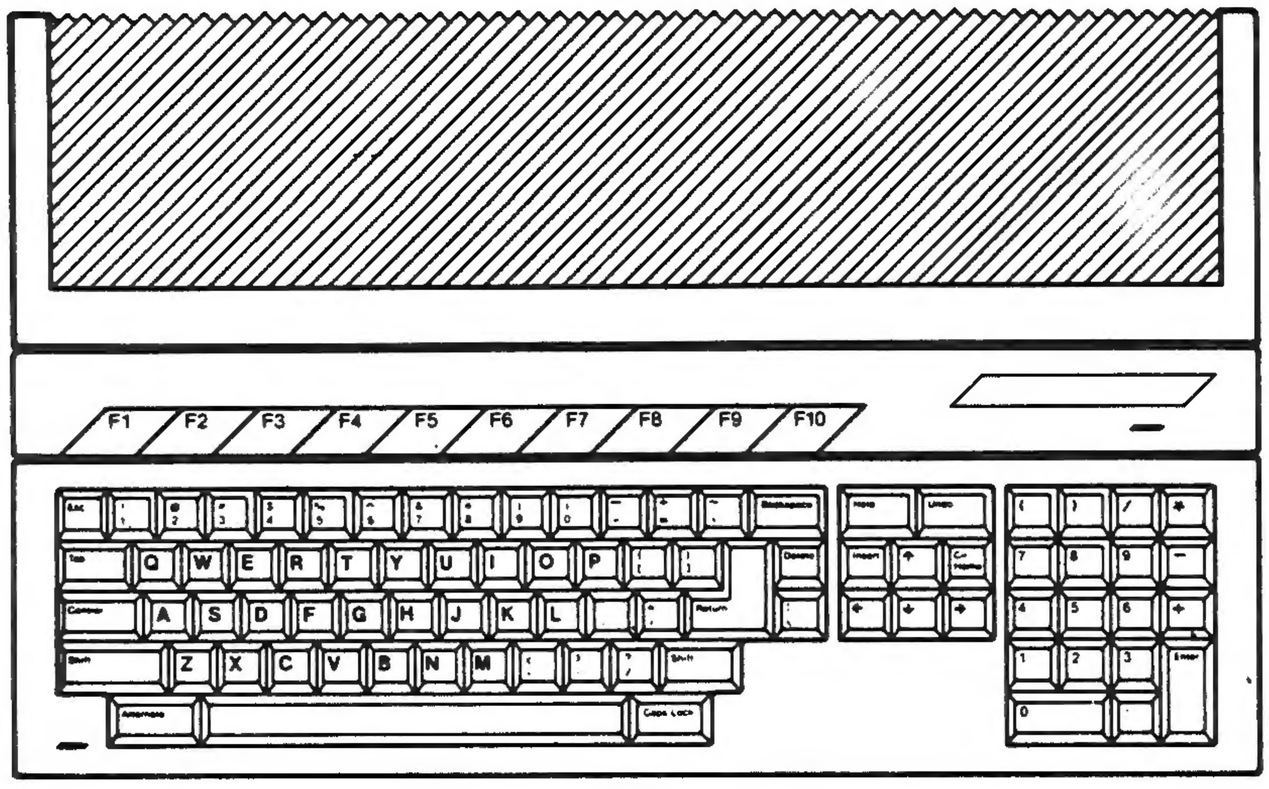


Figure 1-2: 1040STE Upper Case

The left side panels of both machines have slots for the expansion cartridge, two MIDI ports and two game controllers.

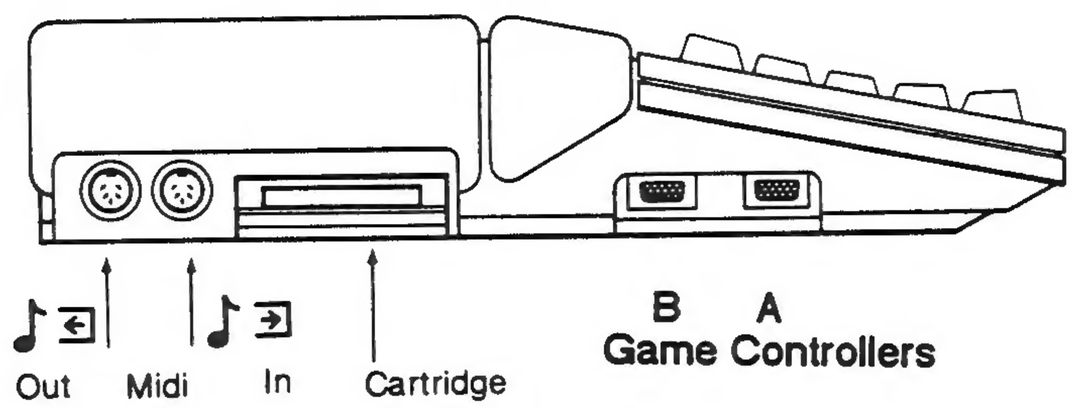


Figure 1-3: STE Left Side Panel

The right side panel has a slot for the floppy disk drive.

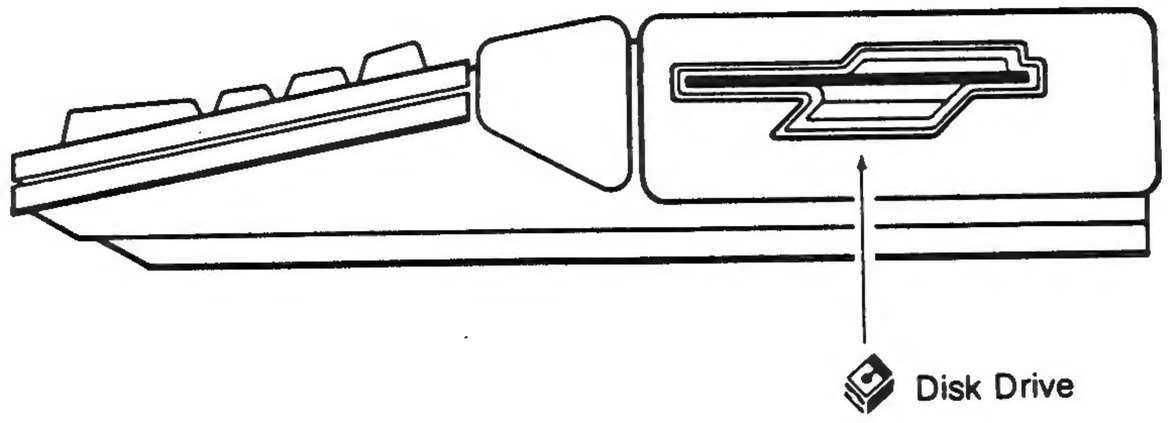


Figure 1-4: STE Right Side Panel

The STE back panel contains (left to right) the modem (RS232) connector, printer connector, hard disk/DMA connector, external floppy disk connector, television output, monitor connector, power switch, stereo output (right and left), AC power input, and reset button. (see **Fig. 1-5**)

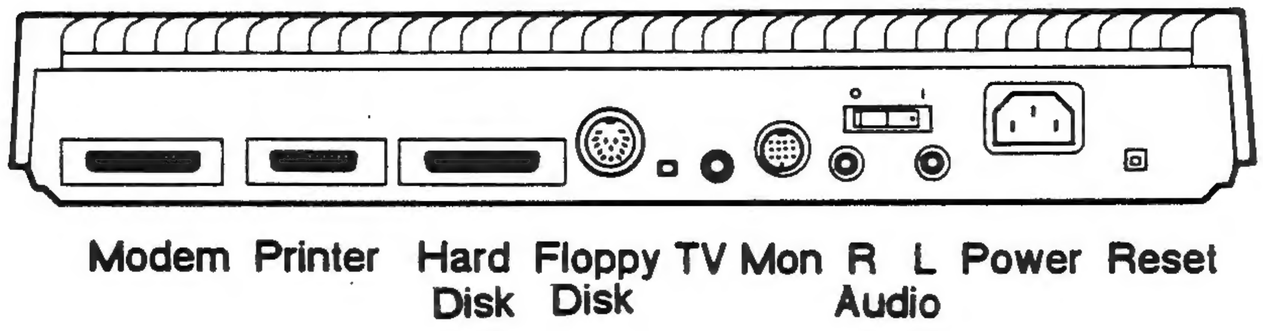


Figure 1-5: STE Back Panel

1.3 POWER SUPPLY

The 520STE and 1040STE have an integral switching power supply providing +5V and +12V. There is a 2A fuse. Voltage should be adjusted to 5.1V. The power supply has overcurrent protection; if the fuse is blown, a catastrophic failure is likely, such as shorted primary.

Power Supply Rating

Current out:	3A at 5V, 0.9A at +12V
Max. power in:	33.5W

Typical (in system) Demand:

Typical current:	1.75A at 5V, 86 mA at +12V
Max. current:	2.2A at +5V, 90 mA at +12 (during disk access)

1.4 NEGATIVE SUPPLIES

The STE motherboard contains two small switching voltage regulators (the TL497 or equivalent) that are used to provide additional voltages.

U204 is used to generate the positive and negative voltages for the RS232C line drivers. These voltages are normally ±12 VDC.

U205 is used to generate a -5 VDC supply for the audio subsection. This output is heavily filtered to reduce the switching noise that might otherwise appear in the audio output.

SECTION TWO:
THEORY OF OPERATION

2.0 OVERVIEW

The 520STE and 1040STE share a common architecture, using the same LSI chip set. The most significant difference is the addition (to the 1040STE) of one bank of 512K of RAM, for a total of 1024K (1,048,568 bytes). Except for the additional RAM, the differences between the 520STE and 1040STE are transparent to software. The hardware can be considered as consisting of a main system (central processing unit and support chips) and several Input/Output subsystems.

2.1 MAIN SYSTEM

- MC68000 running at 8 MHz
- 256 kbyte ROM
- 512/1024 kbyte RAM
- Direct Memory Access Support
- System Timing and Bus Control
- Interrupt Control

2.2 AUDIO/VIDEO SUBSYSTEM

The STE has bit-mapped video display, normally using 32,000 bytes of RAM, relocatable anywhere in memory. There are three display modes available:

RGB, with the ability to be GenLocked:

1. 320 x 200 pixel, 16 color palette from 4096 selections
2. 640 x 200 pixel, 4 color palette from 4096 selections

Monochrome:

3. 640 x 400 pixel, monochrome monitor interface

2.2.1 Audio Output

The STE has a programmable sound chip and 8-bit stereo DMA at 4 playback frequencies.

2.2.2 Television Interface

NTSC, PALI and PALB.

2.3 INPUT/OUTPUT SUBSYSTEMS

- Intelligent keyboard with 2 button mouse/joystick interface
- Parallel printer interface
- RS232C serial interface
- Floppy disk drive and connector for external drive
- Game controller ports
- Hard disk drive interface (ACSI)
- Musical instrument network communication: Musical Instrument Digital Interface (MIDI)

2.4 MICROPROCESSING UNIT

The STE uses the Motorola MC68000 16-bit external/32-bit internal data bus, 24-bit address bus microprocessor, running at 8 MHz.

2.5 GSTMCU

GSTMCU is such an important component that it is involved in nearly every operation in the computer. The functions may be summarized as follows:

CLOCK DIVIDERS takes the 16-MHz clock and outputs 8-MHz, 4-MHz, and 500-kHz clocks.

VIDEO TIMING Blank, DE (Display Enable), Vsync and Hsync are used to generate signals for the video display. There is a Read/Write register in GSTMCU which may be written to configure for 50 or 60 Hz operation or 71 Hz monochrome operation (done by the Operating System).

INTERRUPT PRIORITY interrupts from the MFP and video timing are coded into four levels of priority on outputs IPL0 and IPL1 to the 68000. These levels correspond to no interrupts, MFP interrupts, VSYNC interrupt, HSYNC interrupt.

level 7	reserved
level 6	MFP
level 5	unused
level 4	VSYNC
level 3	unused
level 2	HSYNC
level 1	unused

SIGNAL AND BUS ARBITRATION GSTMCU decodes addresses to generate chip selects to the 6850s, MFP, DMA Controller, Programmable Sound Generator, Memory Controller, and ROMS. It receives signals from the MFP, DMA, Memory Controller, to synchronize data transfer. It arbitrates the bus during DMA transfers to prevent CPU and DMA devices from interfering with each other (see **DMA** below).

ILLEGAL CONDITION DETECTION GSTMCU asserts Bus Error (BERR) if certain conditions are violated, such as writing to ROM, writing to system memory when the processor is in user mode, or if no device responds within 64 cycles of the 8 MHz clock (8µs). For example, if the CPU tries to read from beyond the end of memory, the Memory Controller will not assert DTACK, resulting in a bus error which will terminate the memory cycle.

MEMORY CONTROLLER takes addresses from the address bus and converts to Row Address Strobe (RAS) and Column Address Strobe (CAS). All RAM accesses are controlled by this Atari proprietary chip, which is programmable for up to 4 Megabytes of memory. The Operating System determines how much memory is present and configures the Memory Controller at power-up. The Memory Controller refreshes the dynamic RAMs, loads the Video Shifter with display data, and gives or receives data during direct memory access (DMA). The Memory Controller produces all of the addresses for video, sound, and DMA on the multiplexed address bus. These addresses never appear on the system address bus.

CHIP SELECTS Decodes addresses for RAM and ROM and asserts output signals to enable these devices.

2.6 MAIN MEMORY

Main memory consists of 256 kbytes of ROM and one or two banks (512 kbyte each) of dynamic RAM. In addition, the cartridge slot allows access to 128 kbytes of ROM. All memory is directly addressable. The components of the memory system are: ROM, RAM, GSTMCU and shifter. The Operating System resides mostly in ROM, with optional segments loaded from disk into RAM.

Each bank of RAM in the STE is made up of a pair of 8-bit wide SIMMs to create the 16-bit wide system memory bus. All of the SIMMs in the system must be the same size. It is not possible to mix 256 kbit SIMMs and 1 Mbit SIMMs in the same system. All of the SIMMs used should have the same access time, which can be no greater than 150 ns. It is possible to use 9-bit wide SIMMs, with the hardware simply ignoring the ninth bit.

RAM MEMORY MAP:

000008-000800	System Memory (privileged access)
000800-07FFFF	Low Bank
080000-0FFFFF	High Bank (1040 only)

Note: The first 8 bytes of ROM are mapped into addresses 0-7. These are reset vectors which the 68000 uses on start-up.

The Operating System is located in two 128K x 8 ROM chips.

ROM MEMORY MAP:

E00000 - E3FFFF

2.7 DIRECT MEMORY ACCESS

A single direct memory access (DMA) channel is provided that is shared between the internal floppy disk controller and external devices connected to the ACSI port. Data can be transferred at up to 10 Megabits/sec (1.25 Megabytes/sec) across the 8-bit wide ACSI port.

For DMA to take place, the memory controller is programmed with the starting address at the RAM buffer. The DMA controller is set up to select the source and the number of 512 byte blocks to transfer, and then the FDC or external peripheral is given the command to send or receive data. The entire block of data is then transferred to or from memory without intervention by the CPU. The FDC or peripheral generally asserts its interrupt line to signal the completion of the transfer (and the availability of status information).

To access registers in the FDC or ACSI bus peripherals, the 68000 talks through the DMA chip. The state of two address lines that are generated by the DMAC is set by writing to the DMA control register. Then a 68000 read or write cycle causes the corresponding cycle on the peripheral side of the DMAC.

2.8 MULTI-FUNCTION PERIPHERAL CONTROL

2.8.1 Interrupt Control

The 68901 MFP can generate up to 16 interrupts, 8 internally and 8 from external sources. Each interrupt can be masked off or disabled by programming the MFP. The 8 inputs are also directly readable by the CPU. When the MFP receives an interrupt internally, if the interrupt is enabled, MFPINT will be driven low. When the CPU is ready to respond, it signals interrupt acknowledge (FC2-FC0 high, A3-A1=6, and R/W low) and GSTMCU will assert the MFPs IACK signal (interrupt acknowledge). The MFP will assert DTACK and put a vector number on the data bus, which the CPU will read and use to calculate the address of the interrupt routine.

The interrupts controlled by the MFP are: monochrome monitor detect (MONOMON), RS232 (including CTS, DCD, RI), disk (FDINT and HDINT), parallel port BUSY, display enable (DE, equals the active part of a display line), 6850 IRQs for keyboard and MIDI data, and MFP timers.

Not all I/O operations use interrupts. The CPU can also poll the MFP while waiting for an operation to complete or to check the current status.

2.8.2 MFP Counter/Timers

The MFP clock runs at 2.4576 MHz. The MFP contains four timers:

Timer A Reserved for application software used in the original ST. In the STE, its external event input is used to count DMA sound subsystem cycles.

Timer B External input can be used to count horizontal display lines.

Timer C Reserved for use by the operating system as a periodic interrupt (nominally 200 Hz when running TOS).

Timer D Baud rate generator for the MFP's RS232 port. Its output is used to drive both the receiver and transmitter clock inputs. It will normally be programmed to be 16 times the desired asynchronous baud rate.

2.9 AUDIO/VIDEO SUBSYSTEM

The video subsystem consists of the video display memory (an arbitrary block of RAM starting on any word boundary), the GSTMCU, a graphics control chip (Video Shifter), some discrete components to drive the video output, and an RF modulator. The audio subsystem consists of a Programmable Sound Generator chip, DMA sound circuit, and a programmable mixer (LMC 1992).

2.9.1 Video Shifter (GSTShifter)

There are 16 color palette registers in the shifter. All 16 may be used in low resolution, 4 may be used in medium resolution, and only one is used in high resolution (actually, only bit 0 of register 0 is used for inverse/normal video). Each palette is programmed for 16 levels of intensity of red, blue, and green, so there are 16 x 16 x 16 = 4096 colors possible. For a given pixel, the color which is displayed is taken from the palette pointed to by assembling the bits from each logical plane (see description of video display memory below). The shifter will output the red, green and blue levels specified by the palette. Note that there are four outputs for each color. Each output is either on or off. Thus, the number of possible output levels is 2 to the 4th power = 16 levels. The four outputs are summed through a resistor network to proportion the voltage level to give 16 equal steps. In monochrome mode, the color palettes are bypassed and there is a separate output.

2.9.2 Video Display Memory

Display memory is part of main memory with the physical screen origin located at the top left corner of the screen. Display memory is configured as 1, 2, or 4 (high, medium, or low resolution) logical planes are interwoven as 16 bit words into contiguous memory to form one 32,000-byte physical plane starting at any word boundary. The starting address of display memory is placed in the Memory Controller's Video Base Address register by the Operating System or application. The Memory Controller will load display information into the Video Shifter 16 bits at a time, and the Video Shifter will decode this information to generate a serial display stream. In monochrome mode, each bit represents 1 pixel on or off. In color, bits are combined from each plane to generate the correct level of red, green and blue.

For example, in low resolution (4 planes) 4 words are loaded into the Video Shifter for each word (16 pixels displayed on the screen. The Video Shifter combines bit 0 from each word to form a four bit number (0-15), and takes the color from the palette referenced by that number (e.g., 01001 = 5, use color from palette register 5) and outputs those levels, then takes bit 1 from each plane and outputs the color from the palette referenced by those 4 bits, etc.

2.9.3 GSTMCU

GSTMCU provides timing control to the Memory Controller, video output, and monitor/RF output. VSYNC input to the Memory Controller causes the starting address of the display memory to be reloaded into the address counter during vertical blanking. DISPLAY ENABLE (DE) tells the Memory Controller and Video Shifter that a display line is being scanned and data should be loaded into the Video Shifter. BLANK shuts off the video output from the Video Shifter during periods when the scan is not in a displayable part of the screen. VSYNC and HSYNC both go to the monitor output and RF modulator. These signals synchronize the monitor or TV vertical and horizontal sweep to the display signal.

2.9.4 Memory Controller

In addition to the inputs from GSTMCU mentioned above, there are two output control signals associated with video. DCYC strobes data from the display memory into the Video Shifter. CMPCS (color map select) is active only when changing the color attributes in the color palettes.

2.9.5 Sound Synthesizer

The YM2149 Programmable Sound Generator (PSG) produced music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). The clock input is 2 MHz; the frequency response range is 30 Hz to 125 kHz. There are three sound channels output from the chip, which are mixed and sent to the monitor speaker.

The PSG is also used in the system for various I/O functions relating to printer port, disk drive, and RS232.

2.9.6 Video Interface

The three types of video output interface provided by the STEs are analog RGB and monochrome, composite and modulated RF. The presence of a monochrome monitor is detected by the MONOMON input (when a monochrome monitor is connected, it will be TTL low). The possible displays are:

MONOCHROME: single emitter follower amplifier driving the output of the Video Shifter.

RGB: resistor network sums outputs for each color. The three colors each have an emitter follower amplifier to drive output.

COMPOSITE: the outputs of the emitter followers are input to the modulator box, where the vertical and horizontal sync signals are added to form the composite signal.

TELEVISION: the composite signal is modulated onto an RF carrier. The signal is locked onto the color burst frequency by the phase locked loop (PLL). Without the PLL, the colors will shift or dance on the TV screen.

2.10 STE DIGITIZED SOUND

The Atari ST family of computers is equipped to reproduce digitized sound using DMA (direct memory access; that is, without using the 68000). This section provides the information required to understand and use this feature.

2.10.1 Overview

Sound is stored in memory as digitized samples. Each sample is a number, from -128 to +127, which represents displacement of the speaker from the "neutral" or middle position. During horizontal blanking (transparent to the processor) the DMA sound chip fetches samples from memory and provides them to a digital-to-analog converter (DAC) at one of several constant rates, programmable as (approximately) 50 kHz (kilohertz), 25 kHz, 12.5 kHz, and 6.25 kHz. This rate is called the sample frequency.

The output of the DAC is then filtered to a frequency equal to 40% of the sample frequency by a four-pole switched low-pass filter. This performs "anti-aliasing" of the sound data in a sample-frequency-sensitive way. The signal is further filtered by a two-pole fixed frequency (16 KHz) low-pass filter and provided to a National LMX 1992 Volume/Tone Controller. Finally, the output is available at an RCA-style output jack on the back of the computer. This can be fed into an amplifier, and then to speakers, headphones, or tape recorders.

There are two channels which behave as described above; they are intended to be used as the left and right channels of a stereo system when using the audio inputs of the machine. A monophonic mode is provided which will send the same sample data to each channel.

The stereo sound output is also mixed onto the standard ST audio output sent to the monitor's speaker. The ST's GI sound chip output can be mixed to the monitor and to both stereo output jacks as well.

2.11 GENLOCK AND THE STE

The ST (and STE) chip set have the ability to accept external sync. This is controlled by bit 0 at FF820A, as documented in the ST Hardware Specification. This is provided to allow the synchronization of the ST video. In order to do this reliably the system clock must also be phase-locked (or synchronized in some other way) to the input sync signals. No way to achieve this was provided in the ST. As a result, the only GENLOCKs available were internal modifications (usually for the MEGA).

The STE, on the other hand, allows this to be done without opening the case. To inject a system clock ground pin three (GPO) on the monitor connector and then inject the clock into pin 4 (mono detect). The internal frequency of this clock is 32.215905 MHz (NTSC) and 32.084988 MHz (PAL).

Note: DO NOT SWITCH CLOCK SOURCE WHILE THE SYSTEM IS ACTIVE.

As a result the GPO is no longer available.

MONITOR INPUTS:

HSYNC	TTL level, negative, 3.3k ohm.
VSYNC	TTL level, negative, 3.3k ohm.
Monochrome	Digital 1.0 Vpp, 75 ohm.
RGB	Analog 0-1.0 Vpp, 75 ohm.
Audio	1 Vpp, 1k ohm.

Monitor

1 - Audio Out
2 - Composite Video
3 - General Purpose Output
4 - Monochrome Detect
5 - Audio In
6 - Green
7 - Red
8 - +12 Volt Pullup
9 - Horizontal Sync
10 - Blue
11 - Monochrome
12 - Vertical Sync
13 - Ground

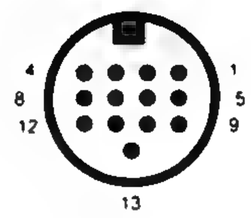


Figure 2-1: Monitor Ports

2.12 INPUT/OUTPUT SUBSYSTEMS

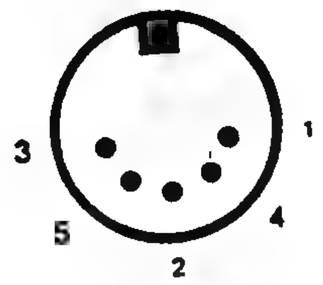
2.12.1 Musical Instrument Communication

The Musical Instrument Digital Interface (MIDI) allows the integration of the STE with music synthesizers, sequencers, drum boxes and other devices possessing a MIDI interface. High speed (31.25 kilobaud) asynchronous current loop serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port). MIDI specifies that data consist of 8 data bits preceded by one start bit and followed by one stop bit.

Communication takes place via a 6850 ACIA. The CPU writes to the 6850 in response to interrupts which are passed from the 6850 to the MFP interrupt controller. The system is interfaced to the outside via two inverters on the transmit side and an LED/photo-transistor chip on the input side. The input signal is also routed around through two inverters to the output connector where it is called MIDI THRU in order to allow chaining of multiple devices on the MIDI bus.

MIDI Out

1 - THRU Transmit Data
2 - Shield Ground
3 - THRU Loop Return
4 - OUT Transmit Data
5 - OUT Loop Return



MIDI In

1 - Not Connected
2 - Not Connected
3 - Not Connected
4 - IN Receive Data
5 - IN Loop Return

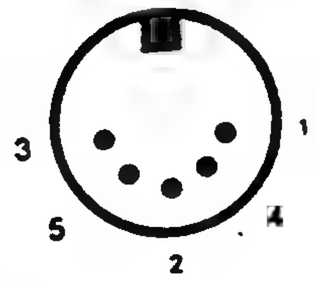


Figure 2-2: MIDI Ports

2.12.2 Intelligent Keyboard

The keyboard transmits make/break key scan codes, ASCII codes, mouse data, and joy-stick data, in response to external events, and time-of-day (year, month, day, hour, minute, second) in response to requests by the CPU. Communication is controlled on the main board by a 6850 device and on the keyboard assembly by the 1 MHz 8 bit HD6301 Microcomputer Unit. The HD6301 has internal RAM and ROM. Included in ROM are self-test diagnostics which are performed at power-up and whenever the RESET command is sent over the serial communication line by the CPU. The MC6850 is read from and written to by the CPU in response to interrupts which are passed to the CPU by the MFP interrupt controller.

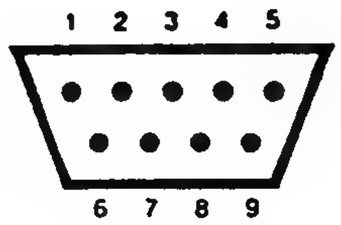
2.12.3 Mouse/Joysticks

The 2 Button Mouse is an opto-mechanical device with the following characteristics: a resolution of 100 counts/inch, a maximum velocity of 10 inches/second and a maximum pulse phase error of 50 percent. The joystick/mouse port has inputs for up, down, left, right, right button, left button. The right button equals the joystick trigger, the left button is wired to the second joystick port trigger. The joystick has four directions (up, down, etc.) and one trigger.

Note: The Atari CX24 joystick cannot be installed during initialization.

Mouse/Joystick

1 - Up/XB
2 - Down/XA
3 - Left/YA
4 - Right/YB
5 - Not Connected
6 - Fire/Left Button
7 - + 5 VDC
8 - Ground
9 - Joy1 Fire/Right Button



Joystick

1 - Up
2 - Down
3 - Left
4 - Right
5 - Reserved
6 - Fire Button
7 - +5 VDC
8 - Ground
9 - Not Connected

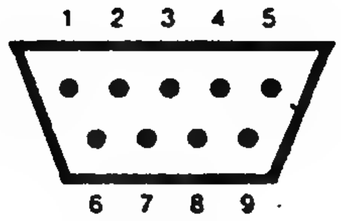


Figure 2-3: Mouse/Joystick Ports

2.12.4 Parallel Interface

The parallel port is primarily intended as a Centronics type printer interface, but can also be used as a general purpose I/O port. Centronics STROBE and BUSY are supported. BUSY is read by the MFP chip. Data and strobe signals are output by the YM2149 PSG chip. Not all Centronics printers are compatible with this port. The current loading on the data lines should not exceed 2.3 mA. (This corresponds to a 2.2k ohm resistor pull-up on the printer side).

The port can be programmed to be input or output. The PSG chip is read directly by the CPU, with GSTMCU doing address decode to provide chip select.

Printer

1 - STROBE
2 - Data 0
3 - Data 1
4 - Data 2
5 - Data 3
6 - Data 4
7 - Data 5
8 - Data 6
9 - Data 7
10 - Not Connected
11 - BUSY
12 - 17 - Not Connected
18 - 25 - Ground

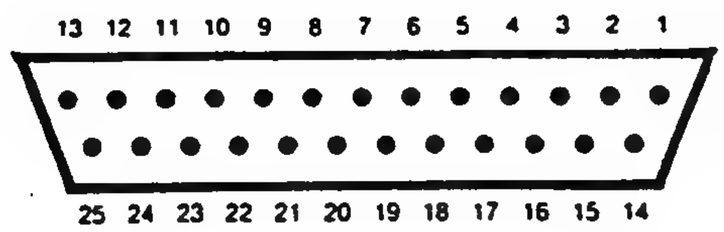


Figure 2-4: Printer Port

2.12.5 RS232C Interface

The RS232C interface provides asynchronous serial communication with five handshake control signals: Request to Send and Data Terminal Ready are output by the PSG chip; Clear to Send, Data Carrier Detect, and Ring Indicator are input to the MFP chip. The MFP contains a USART (Universal Synchronous/Asynchronous Receiver/Transmitter) which handles data transmission and reception. The 2.4576 MHz clock to the MFP is divided by the timer D (pin 16) output of the MFP to provide the basic clock for receiver and transmitter. Data rate of 50 to 19200 bits per second are supported. 1488 line drivers and 1489 line receivers with ±12V supply (supplied by the TL947 DC:DC inverter) meet the EIA RS232C standard for electrical interface.

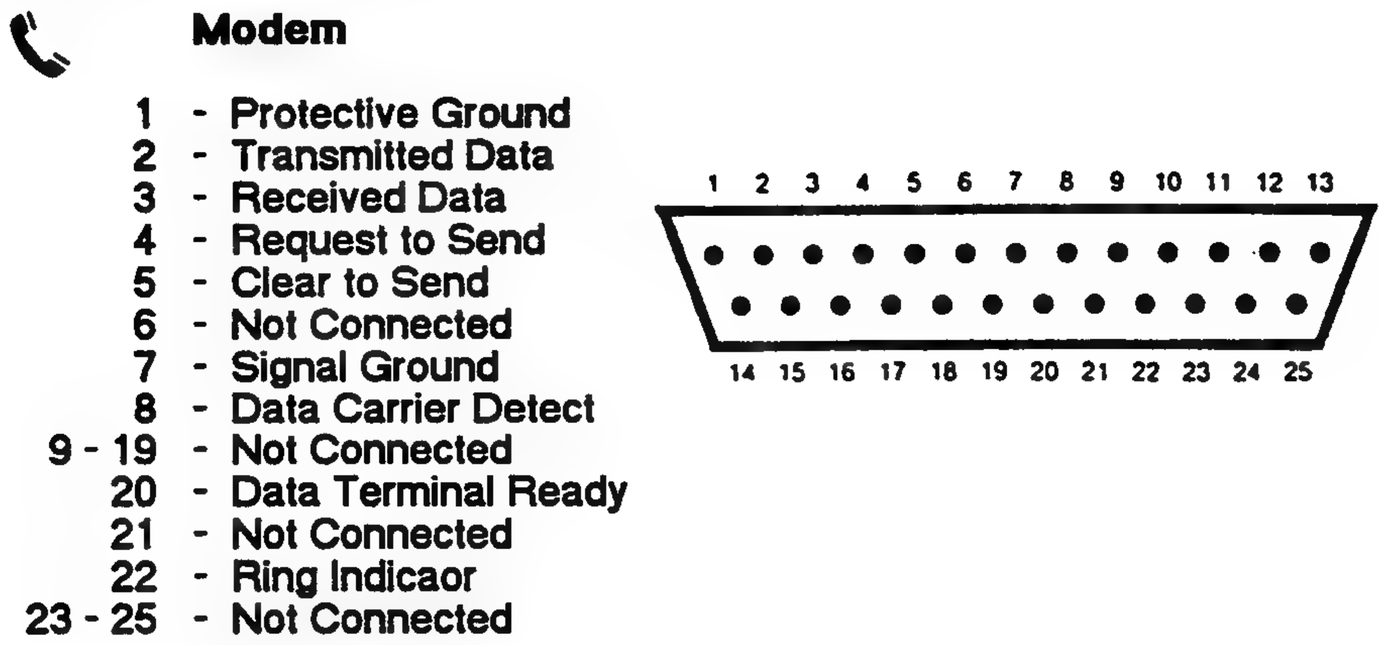


Figure 2-5. RS232 Port

2.12.6 Disk Drive Interface

The STE computers have a built-in floppy disk controller and logic for selecting up to two single or double sided drives. The 1040 STE has one built-in floppy disk drive and provision for one external disk drive. A single 1772 Controller services both drives. Drive and side selection is done by outputs on the YM2149 PSG chip. The CPU reads and writes to the 1772 through the DMA Controller. The 1772 interrupts the CPU on the INTR line, via the MFP interrupt controller. The 1772 accepts high level commands, such as seek, format track, write sector, read sector, etc. and passes data to the DMA Controller (see **DMA controller under Main System**, above, for details on DMA transfer). The 1772 interrupts the CPU when the operation is complete. The CPU is freed from much of the overhead of disk I/O.

Note: Several of the 1772 output signals are externally buffered or inverted. See **Block Diagram**.

Floppy Disk

1 - Read Data
2 - Side 0 Select
3 - Logic Ground
4 - Index Pulse
5 - Drive 0 Select
6 - Drive 1 Select
7 - Logic Ground
8 - Motor On
9 - Direction In
10 - Step
11 - Write Data
12 - Write Gate
13 - Track 00
14 - Write Protect

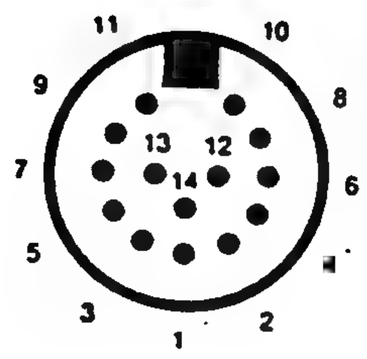


Figure 2-5: Floppy Port

2.12.7 Hard Disk Interface

The hard disk drive interface is provided through the DMA controller. The hard disk controller is off-board and is sent commands via a SCSI-like (Small Computer System Interface) command parameter block. Data is transferred via DMA. Writing to the external controller causes HDCS (Hard Disk Chip Select) to go low and CA1 to go high. DMA transfers are controlled by the external device. When data is available, or the device is ready to accept data, HDRQ will be driven high by the external controller. The DMA chip must respond within 250 nanoseconds with ACK (low) to knowledge that data is on the bus or has been read from the bus. The Memory Controller feeds data to or accepts data from the DMA Controller. Transfers can take place at up to 1 Mbyte/second.

Hard Disk

1 - Data 0
2 - Data 1
3 - Data 2
4 - Data 3
5 - Data 4
6 - Data 5
7 - Data 6
8 - Data 7
9 - Chip Select
10 - Interrupt Request
11 - Ground
12 - Reset
13 - Ground
14 - Acknowledge
15 - Ground
16 - A1
17 - Ground
18 - Read/Write
19 - Data Request

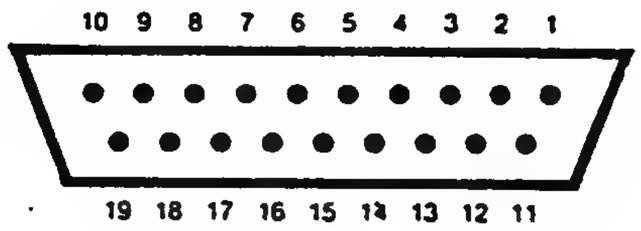
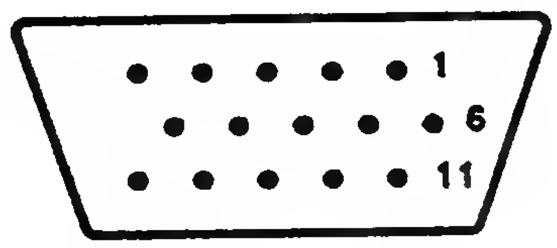


Figure 2-6: Hard Disk Port

Controller A

1 - Up 0
2 - Dn 0
3 - LT 0
4 - RT 0
5 - Pad 0Y
6 - Fire 0
7 - +5 VDC
8 - Not Connected
9 - Ground
10 - Fire 1
11 - Up 1
12 - Dn 1
13 - LT 1
14 - RT 1
15 - Pad 0X



Controller B

1 - Up 2
2 - Dn 2
3 - LT 2
4 - RT 2
5 - Pad 1X
6 - Fire 2
7 - +5 VDC
8 - Not Connected
9 - Ground
10 - Fire 3
11 - Up 3
12 - Dn 31
13 - LT 3
14 - RT 3
15 - Pad 1Y

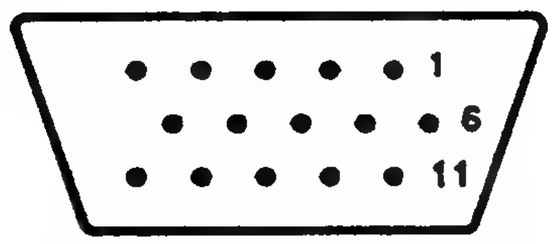


Figure 2-7: Game Controller Ports

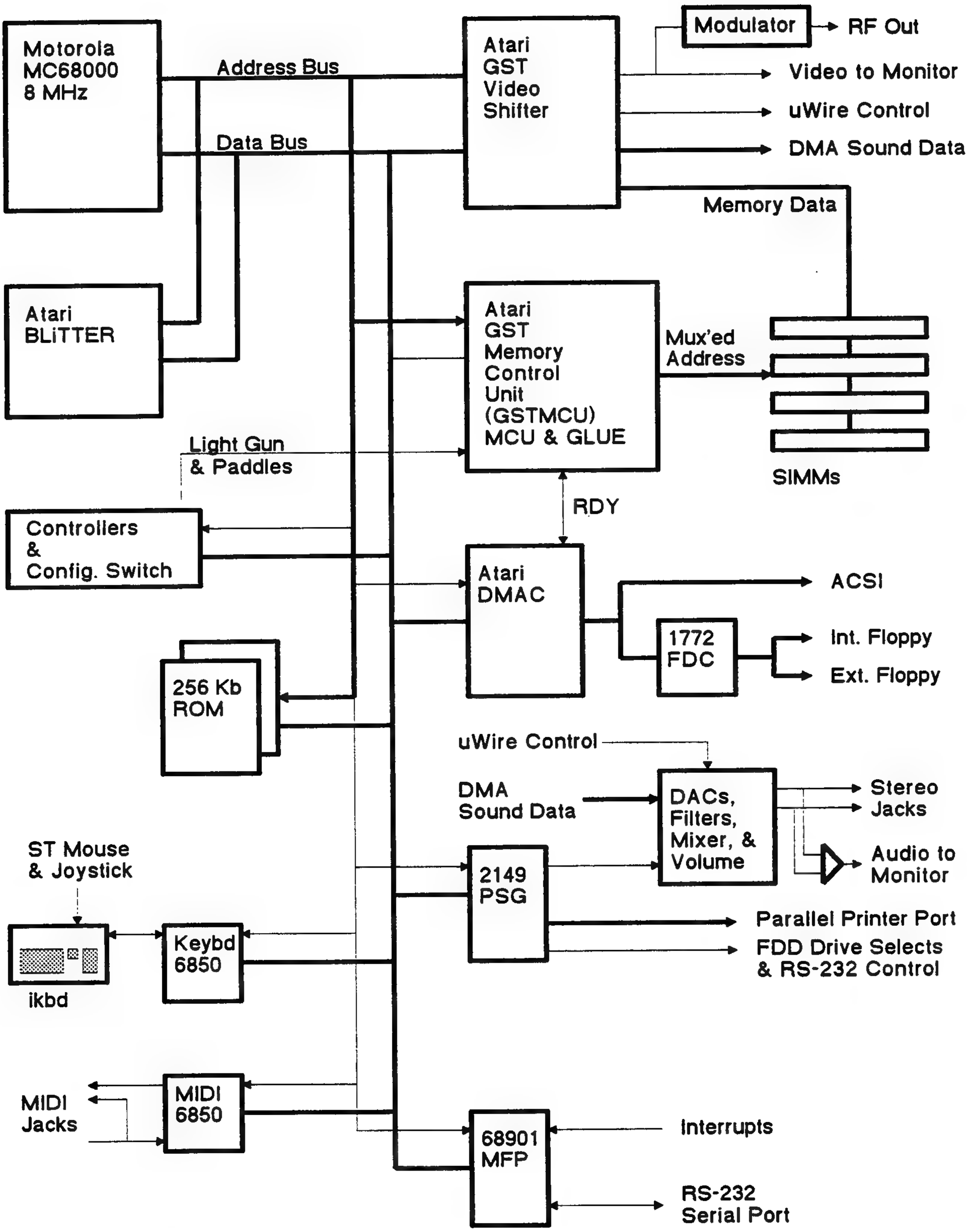


Figure 2-8: STE Functional Block Diagram

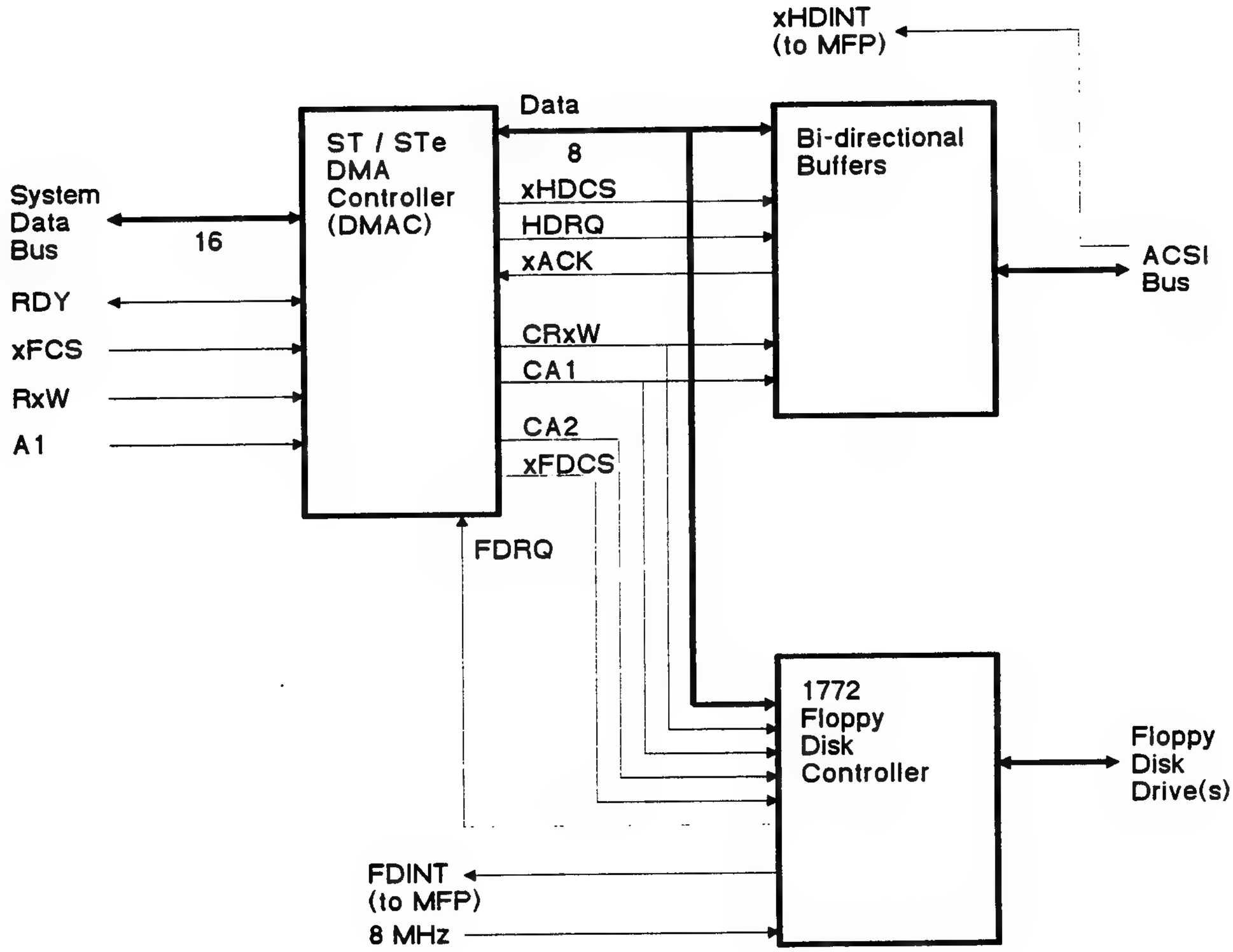


Figure 2-9: STE DMA Block Diagram

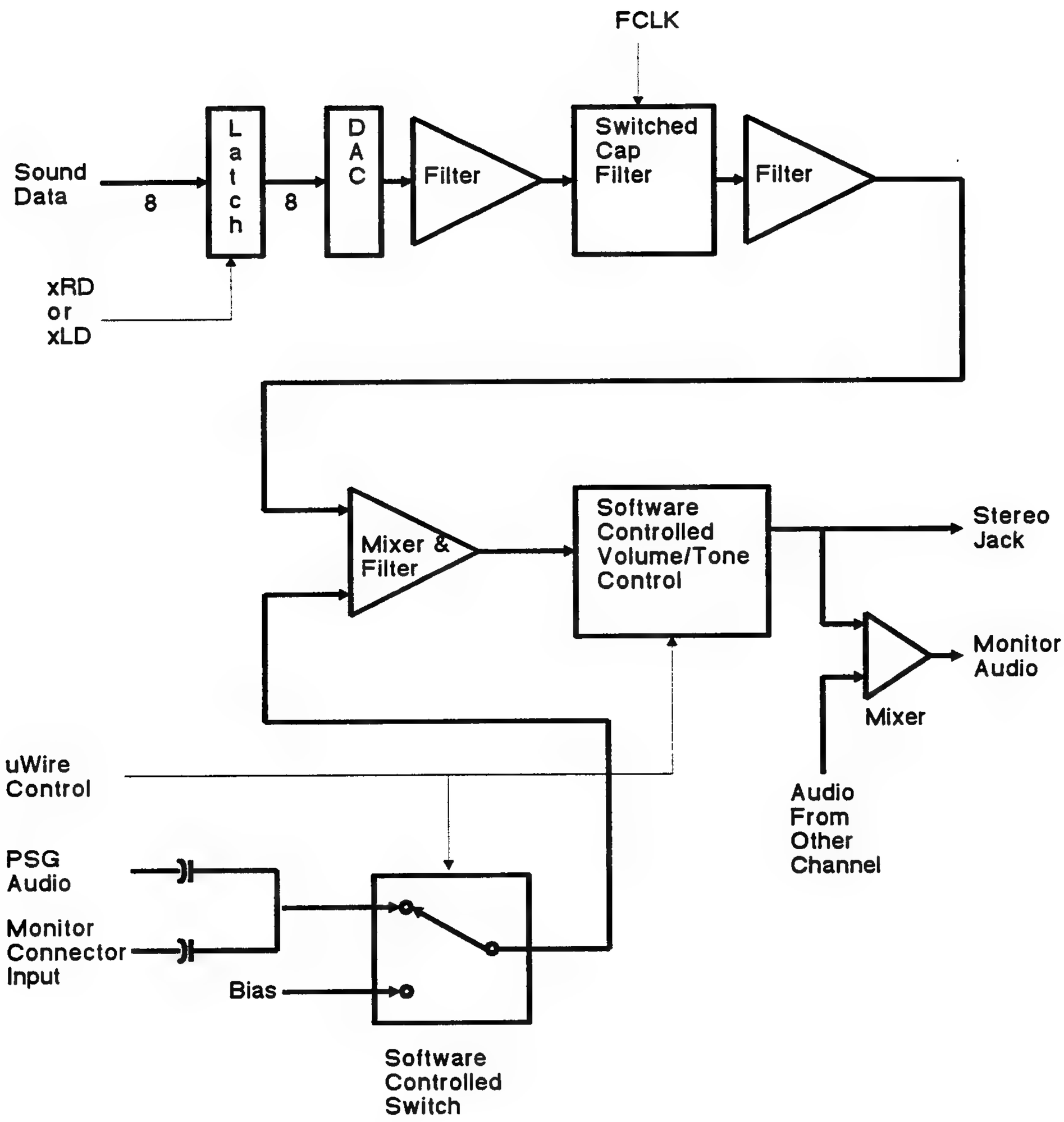


Figure 2-10: STE Audio Block Diagram

2.12.8 Controllers

The controllers allow the integration of the STE with joysticks, paddles, and light gun/pen.

2.12.8.1 JOYSTICKS

Four new joystick ports are added. These ports are controlled directly by the CPU. The current state may be sampled at any time by reading the above locations. Joystick 0 and Joystick 2 direction bits are read/write. If written to they will be driven until a read is performed. Similarly, they will not be driven after a read until a write is performed.

2.12.8.2 PADDLES

One pair of paddles can be plugged into Joystick 0 (Paddle 0). A second set can be plugged into Joystick 1 (Paddle 1). The current position of each of the four paddles is reported at these locations. The fire buttons are the same as for the respective joystick. The triggers for the paddles are read as bits one and two of FF9202 (JOY0 Left and Right).

2.12.8.3 LIGHT GUN/PEN

A light gun or pen can be plugged into Joystick 0. The current position that the gun or pen is pointing to is reported by these registers. The position is accurate to within (X direction only):

4 Pixels in 320 x 200 Mode
8 Pixels in 640 x 200 Mode
16 Pixels in 640 x 400 Mode

Accurate to 1 pixel in the Y direction in all modes. Accuracies do not account for the quality of the light gun or pen. Note that the X position is given in pixels for 320 x 200 only. In order to get correct results in 640 x 200 mode this number needs to be shifted left one bit and in 640 x 400 modes this number needs to be shifted left two bits.

2.13 SYSTEM STARTUP

After a RESET (power-up or reset button) the 68000 will start executing at the address pointed to by locations 4-7, which is ROM (GSTMCU maps the first 8 bytes of ROM at E00000 into the addresses 0-7). Location 000004 points to the start of the operating system code in ROM. The following sequence is then executed:

1. Perform a reset instruction (outputs a reset pulse). (RESET.)
2. Read the longword at cartridge address FA0000. If the data read is a "magic number", execute from the cartridge (cartridge takes over here). If not, continue.
3. Check for a warm start (see if RAM locations are valid). If not, initialize the memory controller.
4. Initialize the PSG chip, deselect disk drives.
5. Initialize color palettes and set screen address.

6. If not a warm start, zero memory.
7. Set up operating system variables in RAM.
8. Set up exception vectors.
9. Initialize MFP.
10. Set screen resolution.
11. Attempt to boot floppy; attempt to boot hard disk; run program if successful.
12. If no boot disk, load the desktop ROM on board 256K ROM.

2.14 SYSTEM ERRORS

The 68000 has a feature called exception processing, which takes place when an interrupt or bus error is indicated by external logic, or when the CPU detects an error internally, or when certain types of instructions are executed. An exception will cause the CPU to fetch a vector (address to a routine) from RAM and start processing at the routine pointed to by the vector. Exception vectors are initialized by the operating system. Those exceptions which do not have legitimate occurrences (interrupts being legitimate) have vectors pointing to a general purpose routine which will display some number of bombs showing on the screen. The number of bombs equals the number of exceptions which occurred.

System errors may or may not be recoverable. Errors in loading files from disk may cause the system to crash, necessitating a reset. Verify the diskette and disk drive before attempting to repair the computer.

2.14.1 Number of Bombs and Meaning

2: **BUS ERROR.** GSTMCU asserted bus error.

3: **ADDRESS ERROR.** Processor attempted to access word or long word sized data on an odd address.

4: **ILLEGAL INSTRUCTION.** Processor fetched an instruction from ROM or RAM which was not a legal instruction.

5: **ZERO DIVIDE.** Processor was asked to perform a division by zero.

6: **CHK INSTRUCTION.** This is a legal instruction, if software uses this, it must install a handler.

7: **TRAPV INSTRUCTION.** See Chk instruction.

8: **PRIVILEGE VIOLATION.** CPU was in user mode, tried to execute a 68000 instruction that can only be performed in supervisor mode.

9: **TRACE.** If trace bit is set in the status register, the CPU will execute this exception after every instruction. Used to debug software.

10: **LINE 1010 EMULATOR.** CPU read an instruction which has '1010' as its most significant nibble. Used by TOS for low level graphics software routines.

11: **LINE 1111 EMULATOR.** CPU read an instruction which has '1111' as its most significant nibble. Used internally in earlier versions of TOS, but reserved on STE.

12: **12-23 Unassigned**, should be no occurrence.

24: **SPURIOUS INTERRUPT**. Bus error during interrupt processing.

25-31: **AUTOVECTOR INTERRUPT**. Numbers 4 and 2 are used, others should have no occurrence.

32-63: **TRAP INSTRUCTION**. CPU read instruction which is used to generate a software exception (such as the entry to GEMDOS, VDI, or AES).

64-79: MFP interrupts.

80-127: Reserved for Atari use.

128-255: Unused.

SECTION THREE:
TESTING

3.1 OVERVIEW

This section pertains to the test equipment, diagnostic software, and test procedures used to verify correct operation and repair of the STE computers. The diagnostic cartridge should be used if possible. If the unit gives no display or RS232 output when running the cartridge, see **Section 3.3: Troubleshooting a Dead Unit**.

Since the STE system is quite complex, it should not be expected that this document can cover all possible problems or pinpoint the causes; rather, the intent here is to give a systematic approach which a technician can use to narrow down a problem to its most likely source. Experience in troubleshooting computer systems is assumed. Knowledge of the 68000 processor may be helpful.

Economics will be an important consideration; due to the low cost of the STE computer line, little time can be justified in troubleshooting down to the component level when it may be cheaper to replace the functional sub-assembly.

3.1.1 Test Equipment

The following equipment may be needed to test the STE computer:

- Atari SC1224 or SC1435 RGB Monitor (or similar)
- Atari SM124 Monochrome Monitor (or similar)
- Atari SF354 or SF314 External Floppy Disk Drive
- ST Port Test Fixture, C103589-001 (DMA Test Fixture)
- STE Port Test Fixture, C301153-001 (Genlock Test Fixture)
- RS232 Loop-Back Connector
- MIDI Loop-Back Connector, C302272-001
- STE Test Diagnostic Cartridge, Revision 1.5 or later (p/n C302260-001)
- Blank Double Sided 3.5" Diskettes (2)
- RS232 Terminal (or STE with VT52 emulator)
- RS232 Null Modem Cable (25 Pin Female-Female)

In addition, the following items may be needed to troubleshoot and repair failed computers:

- Two Channel Oscilloscope
- Small Hand Tools
- Spare Parts

3.2 TEST CONFIGURATION

With the power switch off, install the Diagnostic Cartridge with the label facing UP.

> **Important:** if the cartridge does not have the plastic enclosure; BE SURE THE CARTRIDGE IS INSTALLED WITH THE CHIPS FACING DOWN.

Connect cables from STE test fixture into the hard disk port, parallel port, and joystick/ mouse ports. The joystick cables should be plugged in so that, if the fixture ports were directly facing the computer ports, the cables would not be crossed. Plug the RS232 and MIDI loopback connectors into their ports. Plug the color monitor into the monitor output (a monochrome monitor can be used instead).

Make sure the switch on the STE test fixture is in the position marked INT, otherwise the program will not proceed past the initialization.

Power on the unit. Some tests will be run automatically, in a few seconds the menu screen should appear. If the screen appears, skip down to **Section 3.4: ST Diagnostic Cartridge**, below. If not read the next **Section 3.3: Troubleshooting a Dead Unit.**

If the unit is being used as a terminal for a host computer, it should be disconnected from the host before using the diagnostic; otherwise, the host may think someone is logged on, and will send messages which will act like keystrokes input to the diagnostic.

3.3 TROUBLESHOOTING A DEAD UNIT

In the event that the system is correctly configured and powered and no display appears, this is the procedure to use for determining the problem. This assumes elementary steps have been taken, such as checking the LED in the forward left corner of the computer to verify the unit is powered and making sure the monitor is working.

1. Connect a terminal to the RS232 port of the unit under test (U.U.T.). you can use an STE running the VT52 terminal emulator program — see the owner's manual for setting up the VT52. The cable should connect pin 2 (serial out) of the U.U.T. to pin 3 (serial in) of the terminal and vice versa. Connect pin 7 (ground) to pin 7. The terminal should be set up for 9600 bps, 8 bits of data, 1 stop bit, no parity (this is the default condition for the VT52 emulator).

   Insert the Diagnostic Cartridge into the U.U.T., and power on the unit. If the Diagnostic Cartridge messages appear on the display of the terminal, use the diagnostic to trouble-shoot the computer. If not, the computer will have to be disassembled to troubleshoot. Refer to **Section 3.4: STE Diagnostic Cartridge** for information on using the cartridge.

   If no activity is seen on the RS232 port or display, continue with (2) below.

2. Disassemble the computer so that the printed circuit board is exposed (see **section 4. Disassembly**). Power up the computer. Using an oscilloscope, verify the 8 MHz clock to the 68000 CPU. Replace the oscillator if necessary. Then check the HALT pin of the 68000 CPU. It should be TTL high. If so, go on to 3 below. If not, the CPU is halted. The reasons may be: (a) bad reset circuit, (b) double bus error. (c) bad CPU.

Check (a) by observing signal on input of the two inverters on the HALT line. Check (b) by observing BERR of the CPU as the unit is powered on. It should be high always. If there are logic low pulses, some component is malfunctioning and GSTMCU is generating the error. Verify the clocks to GTMCU, tracing back to the Shifter and MC (master clock) if necessary.

If still failing, the CPU is unable to read ROM or there is a component which is not responding to a read or write by the CPU, probably the MFP 68901 or DMA Controller. The MFP should respond to an MFPCS with DTACK. The DMA chip should respond to FCS by asserting RDY. There is no way to check for a bad CPU other than by elimination of the other two possibilities, although a hot CPU (too hot to touch for more than a second) strongly indicates a bad CPU.

3. If the CPU is not halted, it should be reading instructions from the ROM (cartridge, if installed) and data and address lines will be toggling (if not, replace CPU). At this point, there is the possibility that both the video and RS232 subsystems are failing. Verify the output of the MFP chip (pin 8) while powering on the unit with the cartridge installed. If the data is being sent, trace it through the 1488 driver. Note that ±12V is required for RS232. If all looks good, there may be something wrong with the connection to the terminal.

   Verify also the output of the Video Shifter. If using an RGB monitor, check the outputs to the summing resistors for R, G, and B. Note that if BLANK is not going high, no picture will be output. If using monochrome, check the MONO output pin. Also check the input to the MFP, pin 29, MONOMON. Note that if the CPU does not read a low on this signal on power-up, it will cause RGB output on the Video Shifter instead of MONO.

   If the Video Shifter is outputting a signal, but the picture is unreadable, there is probably a problem with the screen RAM. The cartridge should be used to diagnose this problem, with the RS232 terminal as a display device.

3.4 STE DIAGNOSTIC CARTRIDGE

The STE Diagnostic Cartridge is used to detect and isolate component failures in STE computers. This section gives a brief guide to its use with a description of each test, error codes or pass/fail criteria, and recommendations on repair.

3.5 POWER UP SEQUENCE

The diagnostic program performs several tests on power-up. The messages **"Checking Exception Handling"** and **"testing MFP, GSTMCU timing, Video"** will appear, and the screen will appear scrambled for a few seconds before the menu is printed. The screen will turn red (dark background in monochrome) if an error occurs in the initial testing, with a message indicating the failure. The lowest 2 kbytes of RAM is tested on power-up; if a location fails, the error will be printed to the RS232 device. It is assumed that if RAM is failing, the screen may not be readable and program execution will fail because there are no stack or system variables. The program will continue to test RAM and print errors, but no screen will be displayed (the screen may turn red). Repair RAM.

If the keyboard fails, it will be inactivated. The user must connect a terminal to the RS232 port. The diagnostic program looks for keystrokes from the RS232 device.

If the display is unreadable, the RS232 terminal should be used. All messages are printed to the RS232 port as well as on the screen.

3.5.1 Power-Up Initialization Errors

I1 Error in RAM or Data Bus. (Test walks 1 or 0 across data bus.)

I2 RAM Disturbance Error. (Writing to one location alters data in another location.)

I3 RAM Addressing Error. (Test shows bad RAM cell or incorrect address code.)

I4 Memory Configuration Error. (Problem with Memory Controller or RAM.)

I5 RAM Sizing Error. (Incorrect amount of good RAM found.)

I6 Checking Exception Handling. (This message is always printed on power-up initialization. If the system can fetch the vector from RAM and execute the handling routine, the message will be erased later.)

I7 Bus Error Not Service. (If the GSTMCU does not assert the Bus Error signal, this error will occur.)

T0 MFP Timer Error. (One or more of the four timers in the MFP did not generate an interrupt.)

T1 Vertical Sync (GSTMCU is not generating vertical sync in the required time period.)

T2 Horizontal Sync. (GSTMCU is not generating horizontal sync in the required time period.)

T3 Display Enable. (GSTMCU is not generating DE output or the MFP is not generating an interrupt.)

T4 Video Counter Error. (The Memory Controller is not generating the correct address for the display. This will result in a broken-up display in some or all display modes.)

T5 PSG Bus Error. The PSG chip is defective. (Replace chip.)

T6 1772 Bus Error. The 1772 chip is defective. (Replace chip.)

K0 Stuck Key. A key closure was detected while the keyboard self test was executing.

K1 Keyboard Not Responding. A command was sent to the keyboard processor and no status was returned within the allowed time. Verify that the keyboard is connected to the STE. Verify that Pin 4 of J202 is +5 VDC. Verify that Pin 3 of U201 is 500 KHz ±50 KHz. Replace the keyboard, U201, R210, R209.

K2 Keyboard Status Error. The self test command was sent to the keyboard, on completion of the test, the keyboard sent an error status. Replace the keyboard.

3.6 TEST MENU

The normal screen will be dark blue with white letters. The test title and revision number are displayed at the top, with the amount of RAM and keyboard controller revision below, and a test menu below that. To select tests, the user types the keys corresponding to those tests and the **[Return]** key. Many iterations of the test or tests chosen can be run by typing in the number of cycles just before typing RETURN. Typing a zero will cause the test sequence to run continuously. To stop a cycle before completion, hit the **[Esc]** key (there may be some delay in some tests before the test stops). As each cycle completes, the total number of cycles will be displayed on the screen.

3.6.1 Main Menu (Typical)

```
STE Field Service Diagnostic Test Rev. X.X
© 1990, Atari Corp.
XMbytes RAM     Keyboard Revision 2  60 HZ
O.S. Version X USA NTSC

UNATTENDED
R   RAM Test                O   O.S. ROMs                    M   MIDI
S   Serial Port             T   Timing                      D   DMA Port
F   Floppy Disk             P   Printer/Mouse/Joy & Game Ports
G   Short BLiT              Y   Long BLiT

Q   Run all unattended tests (R,O,M,S,T,D,F,P,Y
Z   Run unattended internal tests (R,O,T,F,G

OPERATOR
A   Audio                   C   Color                       K   Keyboard
H   High Resolution         J   Hard Disk Write/Read

E   Examine/Modify memory
B   Set RS232 rate
X   Toggle video output -- 50/60 Hz
?   Help

Enter letter(s) and RETURN:
```

The RAM size, keyboard revision, O.S. version, country (or language), and television standard (PAL or NTSC) are shown.

The 'Q' selection sequences through all the tests which do not require operator interaction. The 'Z' selection sequences through RAM, ROM, Color, Keyboard, and Timing, Audio and short BLiT tests. Selection 'E' enables the operator to examine or modify RAM or hardware registers. 'B' enables the operator to change the baud rate on the RS232 port. Pressing the up arrow increases it, pressing the down arrow decreases it.

Pressing **'?'** or the **[Help]** key brings up a brief synopsis of the cartridge functions.

After a test (or series of tests) completes. the pass/fail status and error report, if any, will be displayed. Press the space bar to return to the menu.

If multiple tests are selected, the sequence can be halted before completion by pressing the **[Esc]** key. At the completion of the current test, the sequence will halt, with the options of either continuing or returning to the menu. In some cases there will be considerable delay before the current test completes and the keystroke is detected.

3.7 RAM TEST (R)

RAM is tested in three stages: low 2 kbytes, middle (up to 64K), and from 64K to top. The test patterns used are: all 1's, all 0's, a counting pattern (data = low word of the address), reverse counting pattern (data = complement of address low word). The counting pattern is copied from the top and bottom of a 32 kbyte buffer into the current 32 kbytes of video RAM to a new area, verifies the pattern, and repeats the test, until the top of RAM is reached. Finally, addressing at 64K boundaries is checked by writing unique patterns in the last 256 bytes of each 64K block.

If an error occurs, the error code is displayed, followed by the address, data written, data read, and the bits which did not agree.

E.g.: "R2 45603E W: 603E R: 613C bad bits: 1,8"

3.7.1 RAM Error Codes

Except where noted, repair by replacing the RAM chip corresponding to the indicated bit(s).

R0 low memory failed while setting up to run test.
R1 failed walking 1s or 0s.
R2 failed address (counting pattern).
R3 failed 64K boundary test. Probable failure in GSTMCU.
R4 failed while displaying area tested (video RAM).

3.8 ROM TEST (O)

This test reads the configuration bytes of the operating system to determine the version, language/country, and TV standard (PAL or NTSC). All bytes from operating system ROMs are then read and the checksums and CRCs (cyclic redundancy check) are calculated. The configuration byte is then read to determine the language and version of the ROM. The correct checksum and CRC is then read from a look-up table. The unit fails if the values found do not match the values from the look-up table.

Incorrect checksums are indicated by a message. If an error is displayed, replace the corresponding ROM.

New versions of TOS will not cause this test to fail since the calculated CRC is compared with a value found in the new TOS ROMs and is independent of a fixed look up table.

3.9 COLOR TEST (C)

There are four screens in this selection. The first two are used to verify the color circuitry, the third verifies the vertical scrolling circuit, and the fourth verifies horizontal scrolling.

Screen One: red, green, blue, and white color bands are shown. Each band consists of 16 levels of intensity. All 16 color palettes are represented, each palette is a vertical strip across the screen (strips should not be discernible, but each color should be a straight line across the screen). Because of the tight timing involved, keystroke interrupts will cause the display to jitter.

Screen Two: This is the same as screen one except cyan, magenta, yellow, and white color bands are shown. These colors are formed by adding together two primary colors (blue + green, blue + red, red + green). The operator should see that there are no gaps or missing scan lines in the display. If lines are missing, check the three outputs on the Video Shifter for that color, and verify the values of the resistors on the output. Too low a brightness setting on the monitor will cause the monitor not to distinguish between fine levels, making it appear there are only four levels being output.

The Video Shifter has four outputs for red (R0, R1, R2, R3), green (G0, G1, G2, G3) and blue (B0, B1, B2, B3). each of these quadruples is summed together by a resistor network to give 16 levels of intensity for each color, depending on which of the outputs are on. The values of the resistors give different weight to each output. The values of the resistor at R0 is twice that of R1, which is twice that of R2, etc. This allows us to get 16 equal steps on the summed outputs. For example, R0 on and R1, R2 and R3 off = 1/16. R0 off, R1, R2 and R3 on = 15/16. This signal then passes through a transistor amplifier, and from there to the video monitor connector.

3.9.1 Symptoms and Fixes

1. Missing primary color. Check the output of the transistor amplifier. Q402 is blue, Q401 is green, Q400 is red. Look for a staircase pattern (eight levels of intensity). If the signal is there, trace forward to the video connector, if not, trace backward to the Video Shifter, until the faulty component is found.
2. Primary colors present, secondaries missing or incorrect. Replace the Video Shifter.
3. Coarse change in the intensity (not a smooth dark to light transition). Replace Video Shifter or look for a short on the output of one of the three color outputs for the appropriate color.
4. Specks or lines on the screen. This can be caused by bad RAM; if RAM has been tested and is good, replace the Video Shifter.
5. Wavering display, horizontal lines not occurring in the same place every time. The processor may be getting extra interrupts (if the processor is required to handle additional interrupts it will not have time to change all 16 color registers during a horizontal scan time). Examine the MFP interrupt request (pin 32).There should be an interrupt every 126 microseconds (2 display lines) from Display Enable (pin 20). If additional interrupts occur, locate the source: the inputs at pins 22-29 should all be high. If no external (to the MFP) source for the interrupts is found, replace the MFP.

Note: If the keyboard is not connected, the input to the 6850 will be low, causing continual interrupts.

Screen Three: This tests the vertical scrolling function. The screen is divided diagonally, white on top/right, and black on the bottom/left. The screen is scrolled, making more of the screen black, until the entire width of the screen is black. Then the reverse takes place, so that the black portion becomes smaller again. Any break in the border or gaps or sudden shifts indicates a problem in the MCU or RAM.

Screen Four: This tests horizontal scrolling. A series of triangles moves across the screen from right to left. The border should be a straight line and there must be no gaps or sudden shifts. EXCEPT THERE WILL BE SOME SHIFTING ON THE TOP TWO LINES. Any other irregularity indicates a problem in the MCU or RAM.

3.10 KEYBOARD TEST (K)

Two types of tests are run. The keyboard self-test is done first, and if this passes, a screen is displayed representing the keyboard. If multiple tests have been selected, only the self-test is run. The operator presses keys and observes that the corresponding character on the screen changes (reverses background color). The key will also be displayed in the lower half of the screen. The mouse buttons and four directions are also shown on the screen. Connect the mouse, move in any direction, and that arrow will flicker.

Note: It is possible, if pressing keys very rapidly, to leave the representation of the key on screen in a depressed state. This does not indicate a problem with the hardware.

The self-test checks communication between the CPU and the keyboard microcomputer, checks RAM and ROM in the keyboard microcomputer, and scans the keyboard for stuck keys.

3.10.1 Keyboard Error Codes

K0 Stuck key. A key closure was detected while the keyboard self-test was executing.

K1 Keyboard not responding. A command was sent to the keyboard processor and no status was returned within the allowed time. The keyboard needs to be replaced or the communication channel through the 6850 is not functional (see **Sec. 3.5.1**).

K2 Keyboard status error. The self-test command was sent to the keyboard, on completion of the self-test, the keyboard sent an error status. Replace the keyboard.

3.11 MIDI TESTS (M)

This test sends data out the MIDI port, (data loops back through the cable) and reads from the input and verifies the data is current. This also tests the interrupt from the 6850 through the MFP chip. The LED in the loopback cable will blink as data is sent (not all cables have the LED).

3.11.1 MIDI Error Codes

M0 Data not received. Trace the signal from the output of the 6850, through the drivers, loopback cable, and receivers to the input of the 6850. Replace the defective component as found.

M1 Write/Read data mismatch. The data written was not the same as the data read. Replace 6850.

M2 Input frame error. Bad 6850 or bad driver or receiver causing noisy signal.

M3 Input parity error. Bad 6850 or bad driver or receiver causing noisy signal.

M4 Bad 6850 received a byte before the previous byte was read. Input data overrun. Replace the 6850.

3.12 RS232 TESTS (S)

Note: Install Loopback Plug after power up.

First the RS232 control lines are tested (which are tied together by the loopback connector), the data loopback is tested. Data is checked transmitting/receiving using a polling method first, then using interrupts.

Data is transmitted at 300, 600, 1200...19200 bps. Data transmission is performed by the MFP and the 1488 and 1489 driver and receiver chips. Interrupts are a function of the MFP. Control lines are output by the PSG and input on the MFP. Note that this test does not thoroughly test the drive capability of the port. If the unit passes but fails in use, it is likely that the 1488 or 1489 chips are bad.

3.12.1 RS232 Error Codes

S0 Data Not Received. Check signal path, MFP pin 8 to J204 pin 2 via 1488 to J204 pin 3 to MFP pin 9 via 1489.

S1 Data Mismatch. Data read was not what was sent. Check integrity of the signal. May be bad driver, receiver, or MFP.

S2 Input Frame Error. Incorrect time between start and stop bits. Probable MFP failure.

S3 Input Parity Error. Input data had incorrect parity. Probable MFP failure.

S4 Input Data Overrun. A byte was received before the CPU read the previous byte. MFP failure.

S5 No IRQ. CPU did not detect an interrupt by the MFP. MFP or GSTMCU failure.

S6 Transmit Error. MFP transmitter failed.

S7 Transmit Error Interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S8 Receive Error Interrupt. An error condition was created intentionally to cause an interrupt, and the MFP did not respond.

S9 RI/DTR Connection. Signal sent at DTR is not detected at RI.

SA DCD/DTR Connection. Signal sent at DTR is not detected at DCD.

SB RTS/CTS Connection. Signal sent at RTS is not detected at CTS.

3.13 AUDIO TEST (A)

This test requires the operator to decide if the unit passes or fails.

There are two sound generating circuits: the Programmable Sound Generator (PSG) and DMA sound. Both are controlled by the LMC1992 chip and associated circuitry, so if the unit fails both parts of the test, look at the LMC1992 chip first.

3.13.1 PSG Sound

A sound is output on each of the three programmable sound generator channels. The 5/8 sound is a sweep from low to high frequency. Verify that sound can be heard throughout the range, with no dropping of audio level.

3.13.2 DMA Sound

Connect an oscilloscope at the stereo output jacks. The setting should be 1 ms/division, 5 volts/division. There are four parts to this test. After observing the signals, proceed to the next part by pressing the space bar. In each case, the output signal amplitude should go from 0 volts to maximum amplitude in steps.

a. Mono 1 kHz: Both channels output the same signal; it should approximate a sine wave and be 5-6 volts in amplitude.

b. Stereo 1 kHz/500 Hz: Verify that the right and left channels have correct frequencies. As one channel increases in amplitude, the other channel decreases. Maximum amplitude is 5-6 volts.

c. Treble: A 12.5 kHz signal is output on both channels. Maximum amplitude is about 6 volts.

d. Bass: A 50 Hz signal is output on both channels. Maximum amplitude is about 6 volts.

3.14 TIMING TESTS (T)

These tests are run at power-up as well as being selectable from the menu. The MFP timers, the GSTMCU timing for VSYNC and HSYNC, and the Memory Controller video display counters are tested. The video display test redirects display memory throughout RAM and verifies that the correct addresses are generated. Odd patterns may flash on screen as this test is run. There are two tests which check the bus timing for the 1772 and PSG chips. An error message is printed on the screen then the test is run. If the test passes, the message is erased. If not, a Bus Error will occur and the message will remain. If a terminal is connected to the RS232 port, the message will not be erased, but "Pass" will be printed.

3.14.1 Timing Test Error Codes

T0 MFP Timer Error. One or more of the four timers in the MFP did not generate an interrupt on counting down.

T1 Vertical Sync. GSTMCU is not generating vertical sync in the required time period.

T2 Horizontal Sync. GSTMCU is not generating horizontal sync in the required time period.

T3 Display Enable. GSTMCU is not generating DE output or the MFP is not generating an interrupt.

T4 Video Counter Error. The memory controller is not generating the correct addresses for the display. This will result in a broken-up display in some or all display modes.

T5 PSG Bus Error. The PSG chip is defective.

T6 1772 Bus Error. The 1772 chip is defective.

3.15 DMA TESTS (D)

Four sectors (2048 bytes) of data are written to the RAM on the port test fixture via high speed DMA, then read back and verified. This test is repeated many times for RAM addresses throughout the range of RAM.

3.15.1 DMA Test Error Codes

D0 DMA Timed Out. No DMA occurred due to faulty DMA Controller, GSTMCU, or Memory Controller, or the HDINT interrupt was not processed by the MFP. The failure can be isolated by seeing if the DMA Controller responds to HDRQ from the test fixture with ACK. Verify the MFP by seeing that the HDINT input causes an INTR output from the MFP.

D1 DMA Counter Error. The number of bytes transferred was incorrect. The Memory Controller or DMA Controller is bad.

D2 Data Mismatch Error. The data received from the DMA port was not the same as the data sent. Replace the DMA Controller If the problem persists, check the data

lines to the port for opens and shorts. A third possibility is that a defective 1772 is loading the bus.

D3 DMA Controller Not Responding.

3.16 FLOPPY DISK TESTS (F)

In a single test mode, a menu is displayed showing seven options:

1. **Quick Test.** For each disk installed, formats, writes, and reads tracks 0, 1, and 79 of side 0. If double sided, formats and writes track 79 of side 1 and verifies that side 0 was not overwritten. If no disks are installed, checks to see what drives are online and if they are double or single sided. To assure that the drives are correctly tested, the operator should install menu option 6 before calling the test. Once the test is run, the drives become installed, and will be displayed on the menu screen.
2. **Read Track.** Continuously reads a track, for checking alignment with an analog alignment diskette. The choice of track to be read may be input by the operator. If **[Return]** is pressed without entering a number,
3. **Interchangeability Test.** Checks to see if diskettes from two disk drives each can be read by the other disk drive.
4. **Disk Exerciser.** A more thorough disk test; tests all sectors used on the disk for an indefinite period of time.
5. **Copy Protect Tracks.** Tests tracks 80-82, which are used by some software companies for copy protection. Not all manufacturers disk drives will write to these tracks.

   Note: This test is for information only and should not be used to reject a mechanism.

6. **Test Speed.** The rotational speed of the drive is tested and displayed on the screen as the period of rotation. The acceptable range is 196-203 milliseconds. The highest and lowest values measured are displayed. The test stops when any key is pressed.
7. **Install Disks.** Specify how many and what type of disk drives to test.

One additional test which can be performed is testing the write protect detection. Slide the write protect tab to the protected position, and run test #1. You should see **"F5 Write Protected"** displayed if the drive has been installed, or **"Unable To Write Disk"** displayed if the drive has not been installed.

If more than one test is selected from the Main Menu, the Floppy Menu will not appear, but the Quick Test will be selected automatically.

3.16.1 Floppy Disk Test Error Codes

No Floppies Connected – The controller cannot read index pulses. The cable may be improperly connected, or the drive has no power, or the drive is faulty.

F0 Drive not selected. Drive was installed, but failed attempting restore (seek track 0). Check connection of cables, power to drive. Verify that the light on the front of the drive goes on. Listen for the sound of the head seeking (the slide on the diskette should open). If all this occurs, TR0 (pin 23 on the 1772) should go low. If so, check for an interrupt on pin 28 of the 1772. If none, replace the 1772. Else trace the interrupt to the MFP, verify that the MFP responds by asserting INTR. If the drive is not being selected (no light), check the PSG chip. Pin 20 should go low when drive A is selected, and pin 19 should go low when drive B is selected. If not, replace the PSG.

F1 Error of previous version that has been deleted. Error message now says "Error Writing" (or reading or formatting), and displays a more specific error message, e.g., "F9 CRC error."

F2 Error of previous version that has been deleted. Error message now says "Error Writing" (or reading or formatting), and displays a more specific error message, e.g., "F9 CRC error."

F3 Error of previous version that has been deleted. Error message now says "Error Writing" (or reading or formatting), and displays a more specific error message, e.g., "F9 CRC error."

F4 Seek Error. Verify that the STEP, MO, and DIRC outputs from the 1772 are sent to the drive. Probable failure in the 1772, but the drive is also suspect.

F5 Write Protected. Check the write protect tab on the diskette. If OK, verify that the WP input (1772, pin 25) is getting low during the test; if it is then the 1772 is defective; if not, the problem is with the disk drive.

F6 Read Compare Error. Data read from the disk was not what was supposed to be written. Check in the following order: diskette, disk drive, 1772, and DMA Controller.

F7 DMA Error. DMA Controller could not respond to a request for DMA. Replace the DMA Controller. If error persists, check FDRQ while running the test. It should normally be low and go high with each data byte transferred. If stuck high, push the reset button and verify that MR (1772, pin 13) goes low. If not, trace RESET to its source. If MR is OK, but FDRQ is still stuck, replace the 1772.

F8 DMA Count Error. Replace the Memory Controller, if that does not fix it, replace the DMA Controller.

F9 CRC Error. The diskette or disk drive may be bad, else replace the 1772.

FA Record Not Found. The 1772 could not read a sector header. May be a bad diskette, drive or 1772. If the test fails drive A but not drive B, the 1772 is not at fault (likewise fails B but not A).

FB Lost Data. Data was transferred to the 1772 faster than the 1772 could transfer data to the DMA Controller. If DMA Port passes the test, the 1772 is probably bad. The DMA Controller could also be at fault.

FC Side Select Error – Single Sided Drive. The test tried to write both sides of the diskette, but writing side 1 caused side 0 to be overwritten.

FD Drive Not Ready. The format/write/read operation timed-out. Probably a bad disk drive. Verify by checking another drive. Could also be a faulty 1772.

3.17 PRINTER AND JOYSTICK PORT TESTS

The ST Port Test Fixture and STE Game Port Test Fixture must be properly connected for this test.

The port test fixture is used to test the parallel printer port, DMA, and joystick ports. The parallel port test writes to a latch on the test fixture and reads back data. The joystick port tests output data on the parallel port, which is directed through the test fixture to the joystick ports. The keyboard reads the joystick data in response to commands from the CPU. The cables connecting the joystick ports to the test fixture must not be reversed, or the printer and joystick tests will fail.

The game controller port test simulates joystick direction input, fire button input, paddle controller input, and light gun inputs. The STE game port test fixture used the joystick outputs and control lines from the STE Port Test Fixture to generate the signals input to the STE.

3.17.1 Printer/Joystick Error Codes

P0 Printer Port Error. Data read from the printer port was not what was written. Verify that the data lines on the PSG chip (pins 6-13) are toggling when the test is run. If not, run the RS232 test. If the RI-DTR and DCD-DTR errors occur, the chip is probably not being selected. Check if the chip selects are being activated and the 2 MHz clock is present. If the PSG is selected and not outputting signals, replace it. If the data lines toggle, verify continuity. Also verify that J11 (Joystick 0) pin 3 is pulled up. Verify the test fixture is good by testing another computer. If it is OK, replace the PSG

P1 Busy Input Error. The input to the MFP is not being read, or the STROBE output from the PSG is not functioning, or Joystick 0 pin 3 is not connected. If the P0 error also occurs, see handling for that. Otherwise, look for a signal arriving at MFP pin 22 from J5 pin 11. If no signal at J5, the test fixture may be bad. Verify with another computer.

J0 Joystick Port 0. The keyboard input is not functioning. If the busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 , pins 1, 2, 3, 4 to J12 pins 12, 10, 9, 8 respectively.

J1 Joystick Port 1. The keyboard input is not functioning. If the busy input error occurs, fix that first. Otherwise, replace the keyboard. If error persists, check continuity from J11 , pins 1, 2, 3, 4 to J12 pins 7, 5, 4, 3 respectively.

J2 Joystick Time-Out. Joystick inputs were simulated by outputting data on the printer port and routing it via the test fixture to the joystick ports. Joystick inputs are detected by the keyboard and sent to the CPU via the 6850. This error can be caused by printer port failure (code P0), keyboard failure, keyboard-CPU communication line 1, or a faulty test fixture. If the power-up keyboard test passes, this eliminates any problem with keyboard-CPU communication.

J3 Left Button Input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the STE, also check continuity from J10 pin 6 to J12 pin 11.

J4 Right Button Input. If P1 error occurs, fix that first. Otherwise replace the keyboard. On the STE, also check continuity from J10 pin 6 to J12 pin 6.

J5 Aux Joystick Direction. Game controller port (J500, J501) direction bits. U511 is used to drive the input via the test fixture. The hexadecimal data following corresponds to the bits read from latches U510 and U512, where a 1 indicates an error. For example, 0002 indicates an error at J500 pin 3.

J6 Aux Fire Button. Fire buttons are read from U509. Signal is driven via the test fixture from the output of U511.

J7 Paddle. The inputs are driven by either 5V/100 ohms or 5V/1M on the test fixture. This current charges the RC network on the STE, varying the output pulse of the LM556. The pulse width is measured by the GSTMCU chip.

J8 Light Gun. The light gun (XPEN) input is toggled at three points on the screen (the video address counter is used to find the position of the screen). The MCU should return the X/Y coordinates of the screen position. If the XPEN signal is toggling and this error occurs, there is a problem with the GSTMCU.

3.18 MONOCHROME MONITOR (H)

If this test is selected while a color monitor is connected, a message is displayed to connect the monochrome monitor. The CPU waits for an interrupt from the MONOMON input to the MFP, and when received (the operator connects the monochrome monitor), changes the display to high resolution. The display screen will reverse every two seconds. When the operator sees the display is correct, he unplugs the monochrome monitor and re-connects the RGB monitor and the display should return to normal.

3.19 HARD DISK WRITE/READ (J)

This tests the hard disk interface by writing and reading one complete track of the hard disk. It is not intended to test the hard disk drive, but tests the computer DMA circuitry. The test has been found to be more effective than the DMA test for some types of failures; these show up as "Data Compare" errors.

The test program will save the data on the cylinder used for testing and restore the data when the test is done (when "quit" or "park heads" is selected).

> **NOTE:** Always back up the hard disk before running this test. Bad hardware can still destroy the data on the disk.

The test will run until the operator presses the **[Esc]** key. There is no "Pass" condition. A failure will usually show up within a few seconds if it is going to occur at all. The following messages can appear if there is an error:

Controller Not Responding There is no communication between the computer and hard disk. Cycling power on the hard disk may correct this condition.

Operation Timed Out The computer sent a command, which was accepted by the hard disk, but the hard disk did not return a completion code in time.

Command Error The hard disk attempted to execute a command, but an error occurred in the hard disk.

DMA Count Error After completing a data transfer, the byte count of the data in the computer memory controller was incorrect.

Data Compare Error This is followed by the data written to the disk and the data read from the disk. The error is the condition this test was meant to detect. The circuitry involves the custom LSI chips (GSTMCU, Memory Controller, and DMA Controller). The comparison is done by the CPU, and it has found an error in the read/write buffers in memory.

3.20 GRAPHICS CHIP BLiT (G,Y)

Two tests are available for this chip. The "Short BLiT Test" checks the ability of the BLiTTER to move blocks of memory around and perform logical operations on the data. No patterns appear on the screen. If an error is detected, one of the error codes (G1-G12) is displayed.

In the "Long BLiT Test", a triangle is drawn on the screen and rotated 180 degrees until a rectangle is formed. If a color monitor is used, two identical images will be drawn. If an error occurs, a message will appear telling you to replace the BLiTTER.

Corrective action for any error is the same:

a. Verify the jumpers for the BLiT chip are installed correctly.
b. Replace the chip (and if that does not cure the problem, replace the 68000).

3.21 ERROR CODES QUICK REFERENCE

This is a brief summary of all error codes which may occur when running the diagnostic.

3.21.1 Initialization

Error occuring before the title and menu appear. (see **section 3.5.1**)

I1 RAM data line is stuck.
I2 RAM disturbance. Location is altered by write to another location.
I3 RAM addressing. Wrong location is being addressed.
I4 MMU error. No DTACK after RAM access.
I5 RAM Sizing Error. Uppermost address fails.
I6 Bus Error Handling Failed. Bus Error occurred (on purpose), but caused a crash (e.g. System was unable to read the vector from RAM).
I7 Bus Error not detected. Glue not asserting Bus Error or the signal is not reaching the CPU.

3.21.2 Exception (may occur at any time.)

E1 Not used
E2 Not used

E3 Not used

E4 Not used

E5 Not used

E6 Autovector Error. IPLO is grounded or 68000 is bad.

E7 Spurious Interrupt. Bus error during exception processing. Device interrupted, but did not provide interrupt vector.

E8 Internal Exception (generated by 68000).

E9 Bad Instruction Fetch.

EA Address Error. Tried to read an instruction from an odd address or read or write word or long word at an odd address. Usually this error is preceded by a bus error or bad instruction fetch.

EB Bus Error. Generated internally by the 68000 or externally by GSTMCU. Usually caused by device not responding. Displays the address of the device being accessed.

3.21.3 RAM

R0 Error in low memory, possibly affecting program execution.

R1 Error in RAM chip.

R2 Address Error. Bad RAM chip or Memory Controller. Address line not working.

R3 Address error at 64K boundary.

R4 Error during video RAM test. Bad RAM chip.

3.21.4 Keyboard

K0 Stuck key.

K1 Keyboard controller is not responding.

K2 Keyboard controller reports error.

3.21.5 MIDI

M0 Data not received.

M1 Data received is not what was sent.

M2 Data input framing error.

M3 Parity error.

M4 Data overrun. Byte was not read from the 6850 before next byte arrived.

3.21.6 Printer and Joystick/Game Ports

P0 Printer port error.
P1 Busy (printer port input) failed.
J0 Joystick port 0 failed.
J1 Joystick port 1 failed.
J2 Joystick (keyboard controller) timed-out.
J3 Left button line failed.
J4 Right button line failed.
J5 Auxiliary joystick direction (game controller port).
J6 Auxiliary fire button (game controller port).
J7 Paddle (game controller port).
J8 Light gun (game controller port).

3.21.7 RS232

S0 Data not received.
S1 Data received is not what was sent.
S2 Data input framing error.
S3 Parity error.
S4 Data overrun. Byte was not read from the MFP before the next byte arrived.
S5 IRQ. The MFP is not generating interrupts for transmit or receive.
S6 Transmitter error – MFP
S7 No interrupt from transmit error (MFP).
S8 No interrupt from receiver error (MFP).
S9 DTR-RI. These signals are connected by the loopback connector. Changing DTR does not cause change in RI.
SA DTR-DCD. Same as S9 for these signals.
SB RTS-CTS. Same as S9 for these signals.

3.21.8 DMA

D0 Time-out. DMA did not take place, or interrupt not detected.
D1 DMA Count Error. Not all bytes arrived. Possible Memory Controller or GSTMCU error.
D2 Data Mismatch Error.
D3 DMA Controller not responding.

3.21.9 Timing

T0 MFP timers failed.
T1 Vertical sync timing failed.
T2 Horizontal sync failed.
T3 Display Enable Interrupt failed.
T4 Memory Controller video address counter failed.
T5 PSG Bus test. PSG chip is causing a bus error by staying on the data bus too long.
T6 1772 Bus test. 1772 chip is causing a bus error by staying on the data bus too long.

3.21.10 Floppy Disk Drive

F0 Drive offline. Not responding to restore (seek track 0).
F1 Format error. The message will say **"error writing"** (or reading) and display the specific error found.
F2 Error Writing. Gives specific error found.
F3 Error Reading. Gives specific error found.
F4 Seek error.
F5 Write protected.
F6 Data compare. Data read not equal to data written.
F7 DMA error.
F8 DMA count error (GSTMCU).
F9 CRC error.
FA Record not found.
FB Lost data.
FC Side select error.
FD Drive not ready. Timed-out performing the command.

3.21.11 BLiTTER

G1 Halftone RAM (internal RAM in BLiT chip).
G2 Endmask.
G3 Operation.
G4 Halftone Op.
G5 Skew.
G6 Reverse Bit.
G7 Force Extra Source Read.

G8 Smudge.

G9 X Count.

GA Y Count.

GB Time-out.

GC Address Count.

BUS ERROR during BLiT Test – Replace BLiTTER chip.

SECTION FOUR:
DISASSEMBLY/ASSEMBLY

4.1 STE DISASSEMBLY

Use the following procedure to disassemble the STE. Refer to **Assembly Drawing, Section 6.**

4.1.1 Top Cover/Keyboard Removal

1. Turn unit upside down.
2. Remove the 6 screws from the square holes. These fasten the top case to the bottom. If the printed circuit board is to be exposed, or the disk drive is to be removed, also remove the three screws from the round holes. These hold the disk drive in place.
3. Turn the unit upright and remove the top case.
4. Remove the keyboard by unplugging the keyboard harness connector located in the right front corner.

4.1.2 Disk Drive Removal

Remove the the screws in the round holes. Lift the disk drive slightly and unplug the power harness connector and the ribbon cable.

4.1.3 Power Supply Removal

The power supply may be left in place and the upper shield removed in one piece for troubleshooting, as follows:

1. Remove one screw on the right side of the power supply shield. Remove three screws from the back panel EMR shield to the power supply shield.
2. Straighten the two twist tabs.
3. Lift off the power supply shield from the rear.
4. Unplug the wire harness connector in the right front corner of the power supply.
5. Remove two screws at front corners of power supply.
6. Lift the power supply up out of the main assembly.

4.1.4 Removal of Main Assembly from Bottom Case

1. Remove three screws from the front of the shield/printed circuit board assembly.

2. If power supply has not already been removed, remove the two screws securing the power supply to the case at the front corners of the power supply. This can be done by inserting a screwdriver through the holes in the power supply shield or by removing the shield.

3. Lift the assembly up from the front and pull forward.

4.1.5 Removal of Shield from Printed Circuit Board

1. Straighten twist tabs (usually four).

2. Remove copper tape (if present).

3. Lift upper shield straight up.

   Note: Now that the major components are exposed, this is a convenient configuration for troubleshooting. The keyboard and disk drive may be re-connected and placed off to the side if those components are needed.

4. Lift printed circuit assembly away from bottom shield. It may be necessary to pull the twist tabs away from the board slightly.

4.2 STE RE-ASSEMBLY

1. Place insulation panel on Bottom Shield.

2. Place Main Board on top of Bottom Shield over insulator panel.

3. Plug in power supply connector and position power supply with tabs in slots.

4. Align tabs on bottom shield with slots on top shield and fit top shield over main assembly. Twist the tabs to lock in place.

5. Place assembly in lower plastic case.

6. Fasten the power supply to the bottom case at both front corners with two screws. This can be done with the power supply shield in place, using a magnetized screwdriver to hold the screw, or by by removing the shield.

   If power supply shield was removed from main shield, position it over the power supply. Front tabs slide under slots. Twist rear tabs and replace the screw.

   Replace three screws holding back panel EMR shield to the power supply shield.

7. Plug disk drive power and ribbon cables into drive (cables go under shield), and position drive over standoffs.

8. Replace four screws at the front edge of the main assembly.

9. Connect keyboard harness to main board through the opening in the upper shield, and place keyboard on the supporting ribs of the bottom case.

10. Place the top cover over the assembly.

11. Turn over the assembly and replace the nine screws. The three longer screws go in the round holes to secure the disk drive.

    Warning: It is strongly recommended that the computer be retested once in plastic to make sure that the reassembly was done correctly and there are no shorts to the shield.

SECTION FIVE:
SYMPTOM CHECKLIST

This section gives a brief summary of common problems and their most probable causes. For more detail, refer to the section of troubleshooting in this document, or the Diagnostic Cartridge Troubleshooting Guide.

5.1 DISPLAY PROBLEMS

Symptom	Probable Cause
Black Screen	No power (check LED), bad GSTMCU chip, bad Video Shifter. See **Section 3.3: Troubleshooting a Dead Unit**.
White Screen	Video Shifter, GSTMCU, Memory Controller, DMA Controller, 68000. Use diagnostic cartridge with terminal connected via RS232 port.
Dots/Bars on Screen	RAM, Memory Controller, Video Shifter. Use the diagnostic cartridge.
One Color Missing	Video cable or connector. Video summer, buffer, Video Shifter. Check signals with oscilloscope.
Monochrome Monitor Fails to Synch but Color Monitor Okay	Verify that the monochrome monitor detect bit is being grounded when monochrome monitor is plugged in. Check MFP GPIP bit 7; replace MFP.
Scrambled Screen	GSTMCU, Memory Controller. Use diagnostic cartridge.
TV Output Bad	Modulator, phase locked loop. Trace signal with oscilloscope.

5.2 DISK DRIVE PROBLEMS

Symptom	Probable Cause
Disk Won't Boot	Power supply, 1772, DMA Controller, PSG chip, disk drive external ACSI buffer, external HD IRQ lines shorted to ground. See if Select light goes on, if not, check PSG outputs. Listen for motor spinning. If not, check power supply. Swap disk drive or try external drive. If not working, check DMA Controller 1772 with diagnostic chart.
Disk Won't Format:	1772, DMA Controller, disk drive.
System Crash after Loading Files	Data on diskette, disk drive, 1772, DMA, or GSTMCU. Swap diskette, retry. Use diagnostic cartridge to check 1772, DMA Controller, GSTMCU; replace disk drive.

5.3 KEYBOARD PROBLEMS

Symptom	Probable Cause
Red Screen: Keyboard not responding	Bad keyboard, 6850, MFP.

5.4 MIDI PROBLEMS

Symptom	Probable Cause
Red Screen: Error Codes M0, M1, M2, M3, or M4	Bad opto-isolator chip, 6850, inverter (74LS06). See **Section 3.11.1**

5.5 RS232 PROBLEMS

Symptom	Probable Cause
Red Screen: Error Codes S0 through SB	Bad MFP, 1489 receiver, 1488 driver, or PSG chips, ±12 VDC:DC inverting power supply. See **Section 3.12.1**.

5.6 PRINTER PORT PROBLEMS

Symptom	Probable Cause
Red Screen: Error Codes P0, P1:	Bad PSG, MFP chips. See **Section 3.17.1**
Shadow Printing	Bad ASCI port cables, terminator resistors, bad LS244, LS245 drivers.

5.7 HARD DISK PORT PROBLEMS

Symptom	Probable Cause
Red Screen: Error Codes D0, D1, D2	Bad DMA Controller, Memory Controller, 1772 (loading the bus). See **Section 3.15.1**

5.8 DMA SOUND

Symptom	Probable Cause
No Sound	+8V regulator, ±supplies, 1992 Volume Control, R542, R543

SECTION SIX:
DIAGNOSTIC FLOW CHARTS

This section summarizes in diagrammatic form the steps taken in troubleshooting the STE using the diagnostic cartridge. The details of using the cartridge are not shown; this shows the context in which the cartridge would be used, including some problems for which the cartridge would not be useful. Usage of the cartridge is covered in the troubleshooting guide. In general, the user would run all tests, look up errors in the troubleshooting guide, and take the action recommended.

Although a thorough understanding of the system may be necessary in solving some problems, in most cases following the flowchart, reading the documentation on the diagnostic cartridge where necessary, and swapping out the indicated component(s) will result in repair of the problem.

6.1 REPLACEMENT PROCEDURES

Where replacement is indicated, replace the component (if more than one is indicated, replace one at a time) with a known good part. If other components are later replaced, verify whether the first part is good by replacing it in the system once the system has been repaired.

6.2 HANDLING OF INTEGRATED CIRCUITS

Warning: Extreme care should be taken when handling the integrated circuit chips. They are very sensitive to static electricity and can easily be damaged by careless handling. Keep chips in their plastic carriers or on conductive foam when not in use. The operator handling such components should wear a properly grounded ground strap and work on a properly grounded conductive surface.

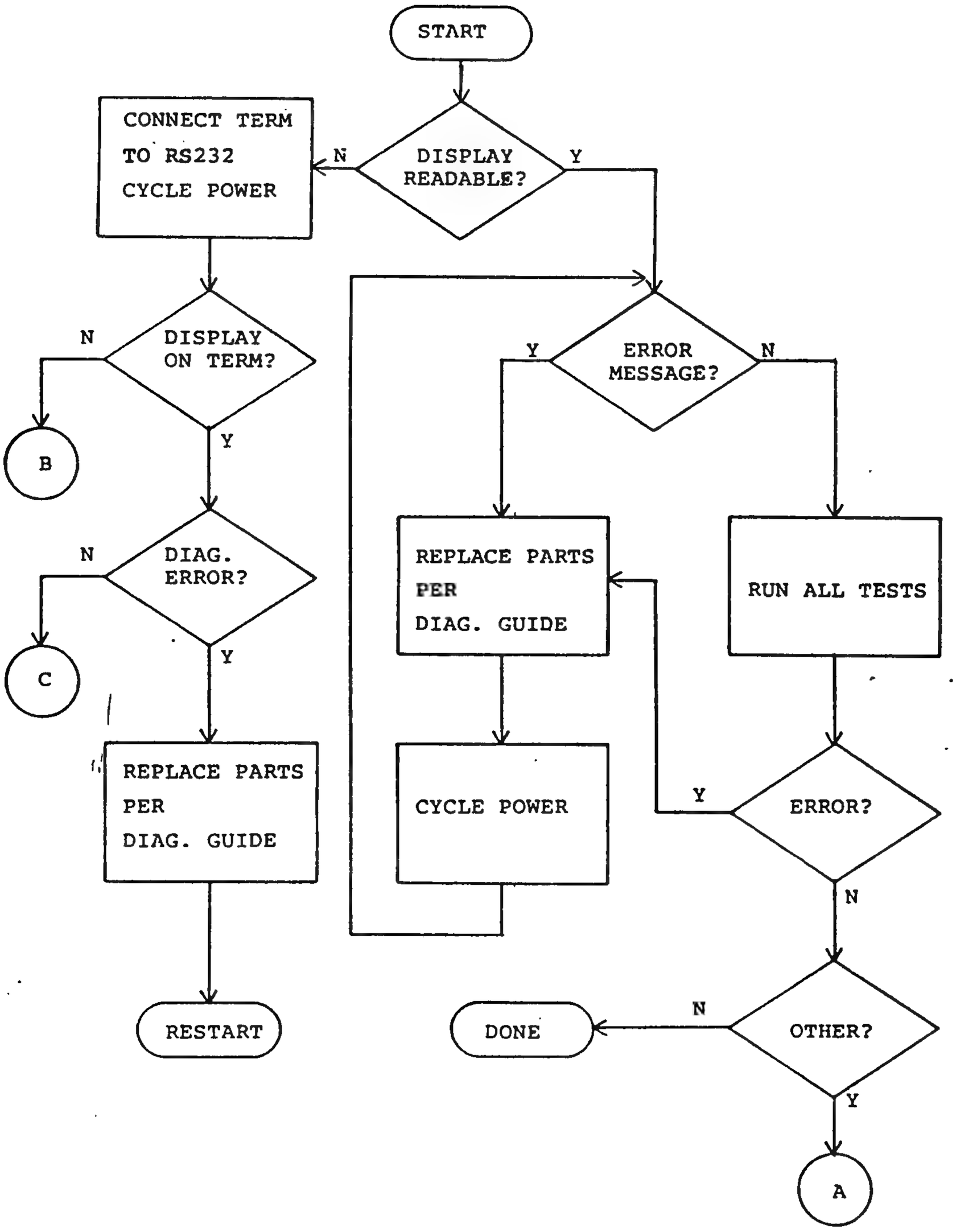


Figure 6-1: STE Diagnostic Flow Chart

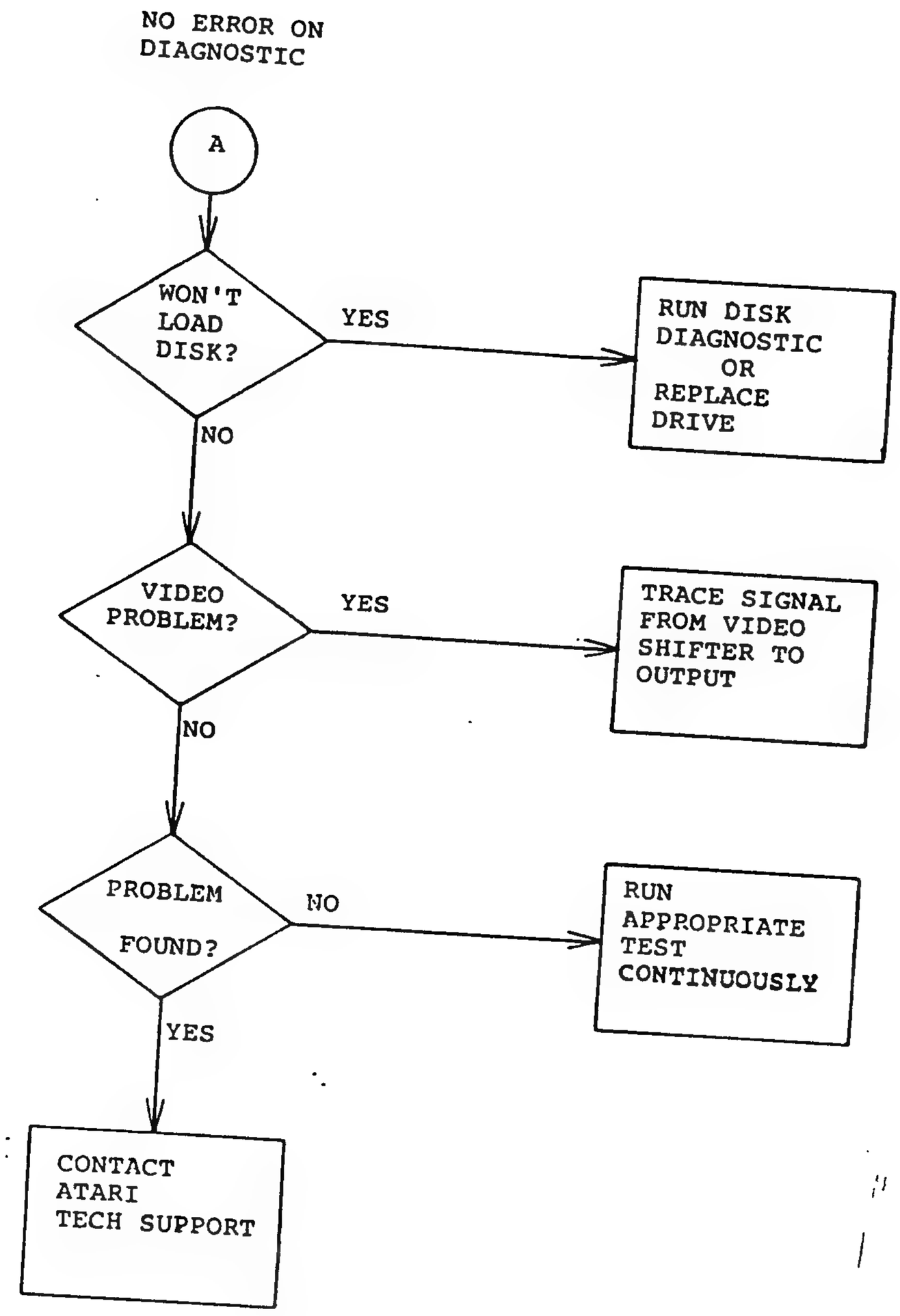


Figure 6-2: STE Diagnostic Flow Chart

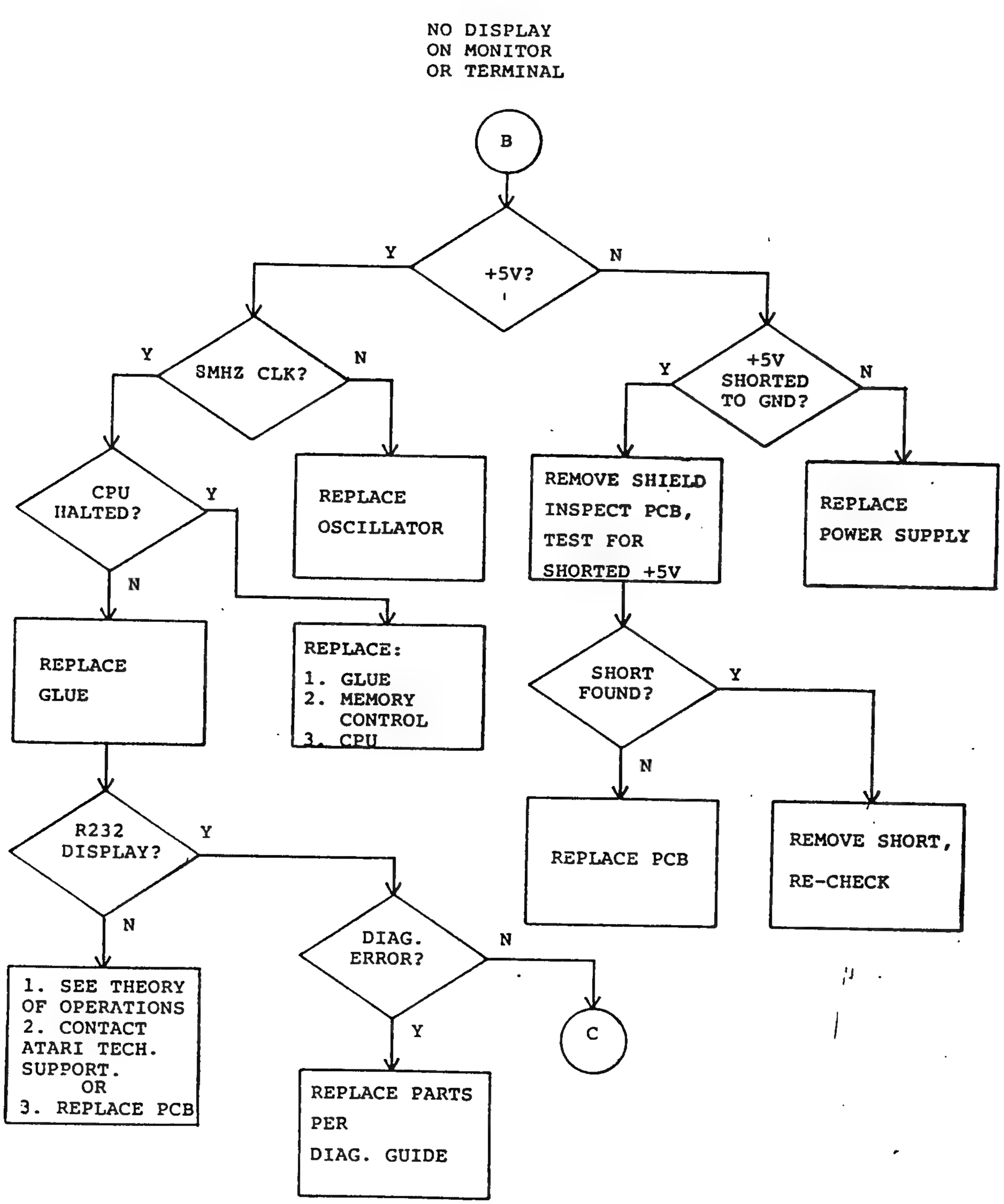


Figure 6-3: STE Diagnostic Flow Chart

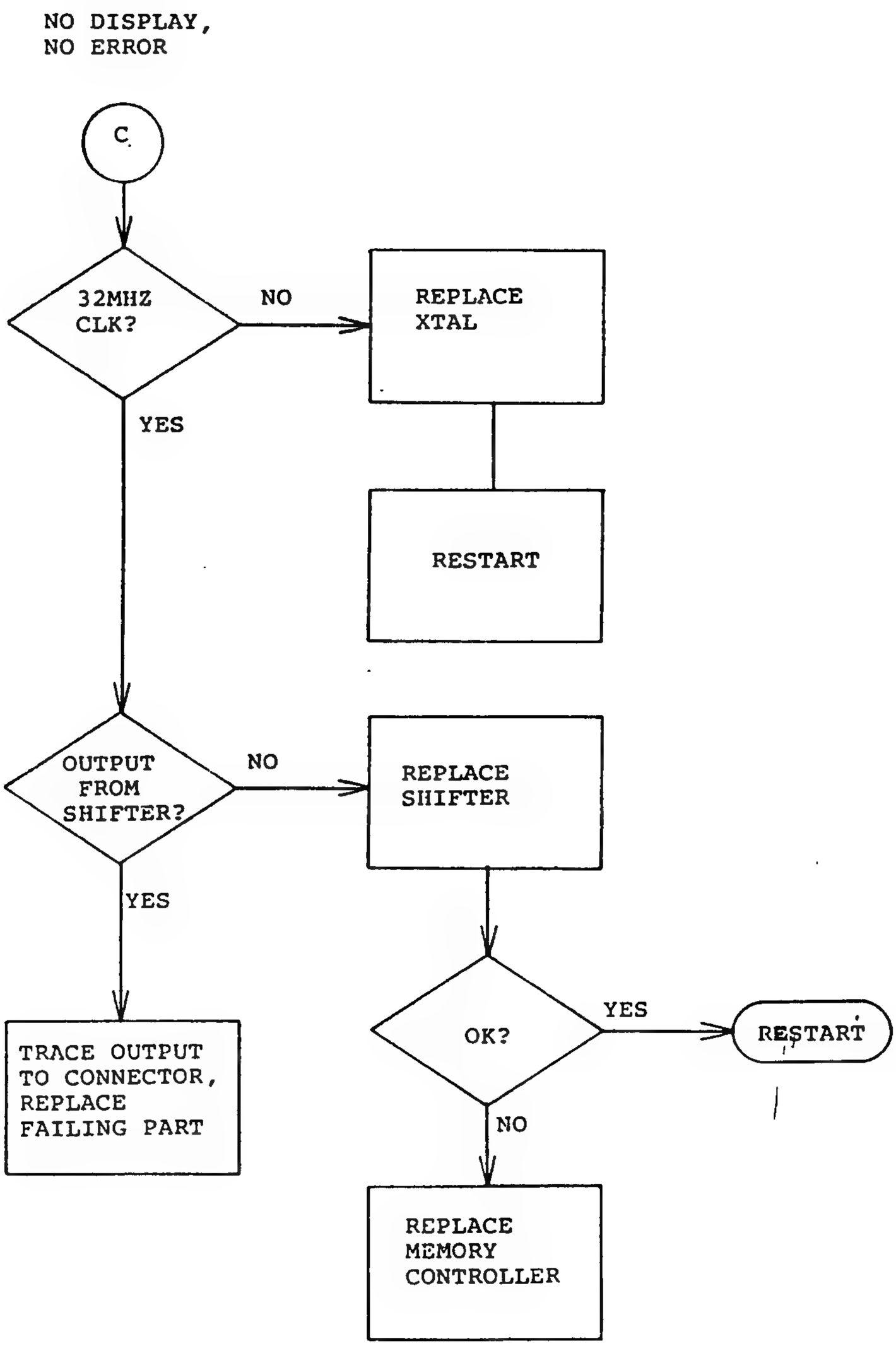


Figure 6-4: STE Diagnostic Flow Chart

SECTION SEVEN:
PARTS LIST

ASSY NO: CA400338-201

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
CA200133-001 1	ASSY CABLE COAXIAL (NTSC)	1
C070349-001	CORD AC WITH POLY BAG	1
CA400607-001	DISK LANGUAGE USA IDD	1
C026406-001	MANUAL OWNER'S	1
C100536-001	MANUAL BASIC MEGA/ST/STE	1
C100971-001	MANUAL PCM1 ENG.	1
C300986-001	MANUAL ADDENDUM STE ENG.	1
CA070025-	MOUSE MEGA/ST/STE	1
CA400339-201	ASSY MAIN 1040 STE W/MOD USA	1

ASSY NO: CA400339-201

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
CA400343-003	ASSY TOP CASE 1040 STE	1
CA400344-001	ASSY BTM CASE NTSC	1
C301430-001	SHIELD REAR STE FCC USA/CAN/GE	1
CA400340-111	ASSY PCB 1040 STE USA W/MOD	1
CA070059-003	ASSY PSU 110V STE USA/CAN	1
CA070057-005	ASSY K/B CAN ST	1
C103704-001	FDD 1MB 3.5" SONY W/LED	1

ASSY NO: SE400340-111

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
CA400329-101	ASSY PCB SUB STE NTSC W/MOD	
CA400366-001	ASSY TOS ROM 1.62 USA STE	U102 - 103
CA400495-001	ASSY SIM 256K x 1 x (8) DIP	U600 - 603

ASSY NO: CA400366-001

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
C301163-002	IC TOS ROM 1.62 USA HI STE	U102
C301164-002	IC TOS ROM 1.62 USA LO STE	U103

ASSY NO: CA400495-001

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
C398152-001	PCB SIMM 256K x 8 DIP STE	1
C101743-002	IC DRAM 256K x 1 120 NS 16P	8
C101207-224	CAP CER .22UF 50V AX	2

ASSY NO: CA400329-101 DESC: PCV SUB ASSY STE W/MODULATOR

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
C300780-001	SCHEMATIC DIAGRAM	
CA070023-009	ASSY CABLE 4P CONN 280 MM	J302
CA070024	CABLE FLAT ASSY 34P	J303
CO70335	BANDAGE PLATE	
CO25993	CRYSTAL 2.4576 MHZ	Y200
C398066-001	OSC 8.010613 MHZ	U303
C398068-001	OSC 32.215905 MHZ	U402
CO19748	IC 555 TIMER 8P	U104
C398739-001	IC DMA CONTL 4140 40P	U300
CO25983	IC YM-2149 SOUND 40P	U202
C025984	IC 68901 MFP 48P	U203
C025985	IC 6850 ACIA 24P	U200,201
C025986	IC MC1488 RS232C DRIVER 14P	U206
C025988	IC PC900 PHOTO COUPLER 6P	U208
CO25989	IC LM556 DUAL PRECISION 14P	U513,514
CO26028-002	IC 1772 FDD CONTROLLER 28P ST	U301
C070447	IC TL497A SW REGULATOR 14P	U204,205
CI00117	IC MC1377 ENCODER 20 PIN	U403
C101609-006	IC 7406 DIP 14P	U210,305

C101610-257	IC 74S257 DIP 16P	U405
C101611-004	IC 74LS04 DIP 14P	U211
C101611-074	IC 74LS74 DIP 14P	U304,306
C101611-086	IC 74LS86 DIP 14P	U209
C101611-164	IC 74LS164 DIP 14P	U900
C101611-244	IC 74LS244 DIP 20P	U307,509,510,512,632
C101611-245	IC 74LS245 DIP 20P	U302
C101611-373	IC 74LS373 DIP 20P	U511
C101643	IC ST BLITTER CUSTOM 68 PIN	U101
C101739-001	IC 1489A RS-232C RECEIVER 14P	U207
C300259-257	IC 74F257 DIP 16P	U405
C300259-374	IC 74374 DIP 20P	U500,501
C300588-001	IC STESHFTR 84P NATIONAL	U401
C398055-001	IC LF347 14P	U504,507
C398056-001	IC MF4-100 8P	U505,506
C398057-001	IC DAC0802 16P	U502,503
C398058-001	IC LMC1992 28P	U508
C398061-001	IC 68000 PLCC 68P	U100
C070734-002	IC LM78L82 VOLTAGE REGULATOR 3P	Q500
34-2N3904	IC TRAN 2N3904 3P	Q400 - 404
C101008-472	RES NET 4.7K 5% 9P BUS	P101-103, 500-502
C070448	RES NET SIP 10K 9P	P104,105,600
C101008-122	RES NET 1.2K 9P	P100
C070157-004	CAP ELEC 47UF 16V RA	C566,567
C398121-001	CAP ELEC 47UF 16V 20% RA	C416
C398069-001	CAP 15UF 25V +/-2 RA TANTL 0%	C420,424,426
C070157-005	CAP ELEC 100UF 16V RA	C423,417
C070157-008	CAP ELEC 470UF 16V RA	C415
C070450-001	CAP ELEC 4.7UF 25V 20% AX NPO	C202,204,205,215
C070450-002	CAP ELEC 10UF 35V 20% RA	C100,542
C070450-008	CAP ELEC 470UF 3 5V 20% AX	C216
C070499-001	CAP ELEC 22UF 16V +-20% AX	C102

C070499-003	CAP ELEC 47UF 16V 20% AX	C508,520,525,529,535 537,541,C543,544,546, 547
C070499-004	CAP ELEC 100UF 16V	C107,110,600,558, 561,564
C070566	CAP ELEC 1UF 50V	C433
C101205-472	CAP ELEC 4700UF 16V AX	C103
C070741-007	CAP MICA 680PF 50V +-5% RA	C526,532,539,548
C101403-102	FILTER NOISE TDK	L200-202,204-207,209-227,511-527, L300-310, 404-409,504-507,509,510
C070241-002	FILTER NOISE *ALT* ZJS5101-02	
C100091-002	FILTER NOISE *ALT* DSS306-55B 102M	
C101403-002	FILTER NOISE *ALT* ZJSR5101-102	
C101404-002	FILTER NOISE *ALT* STB102KB	
C100210	COIL VARIABLE 24UH	L403
C100209	DELAY LINE 3.58 MHZ	DL1
C070119	SW PUSH SP J312U	S100
C100184	RF MODULATOR ST NTSC	ST MOD
C014386-13	SKT UC IUO 32 POS	U102,103
C070120-002	SKT 68P PLCC	U100,101
C070718	PLCC STOPPER 68P	
C100384-001	CONN SKT PLCC 84P STG	U401
C398063-001	UC SOCKET SIMM 30P	U600,603
C070033	CONN DIN 5P MIDE I RIGHT ANGLE	J200,201
C070129	CONN 40P RIGHT ANGLE	J103
C070130-002	CONN DB19S HARD HOOK TYPE	J301
C070131	CONN DIN FLOPPY DISK 14P	J304
C070132-002	CONN DB 25P RS232C HOOK TYPE	J204
C070133-002	CONN D 25B FEMALE RT-ANGLE	J203
C070134	CONN 13P DIN VIDEO	J400
C070445	CONN SINGLE INLINE 6P	J100
C070446	CONN SINGLE INLINE 8P	J202
C398064-002	CONN D SUB 15P 3 ROW FEMALE	J500,501

C398065-001	CONN PHONO RIGHT ANGLE	J502,503
C100287-070	WIRE SOLID AWG26 200MM	

ASSY NO: SB400329-101

PART NUMBER	DESCRIPTION	LOCATION
C060607	DIODE 1N4148	D100,200-203
31-1N914	DIODE 1N914 SIGNAL *ALT* SILICON	
C060629	RES JMPR 0	R405,451,459
C101004-1002	RES MF AX 10K 1%1/4W	R501-504,505,506, 510-515
C101004-1003	RES MF AX 100K 1% 1/4W	R545,546
C101004-1801	RES MF AX 1.8K 1% 1/4W	R507,516
C101004-8201	RES MF AX 8.2K 1% 1.4W	R500,508,509,517
14-5010/A	RES CF 1 5% 1/4W	R211
14-5100/A	RES CF 10 1/4W 5% AX	R542,543
14-5101/A	RES CF 100 1/4W 5% AX	R441
14-5102/A	RES CF 1K 1/4W 5% AX	R102,107,209,220, 300-306,406,413,421, 429,430,440.442,470,541, 540,R520,533,463
14-5103/A	RES CF 10K 1/4W 5% AX	R100,103105,210,525, 527,530,538
14-5105/A	RES CF 1M 1/4W 5% AX	R518,521,528,535
14-5122/A	RES CF 1.2K 1/4W 5% AX	R106,208,213,431
14-5123/A	RES CF 12K 1/4W 5% AX	R101,206,411,416,422
14-5151/A	RES CF AX 150 1/4W 5%	R448
14-5152/A	RES CF 1.5K 1/4W 5% AX	R412,417,424,452
14-5202/A	RES CF AX 2K 1/4W 5%	R408,423,433
14-5221/A	RES CF AX 220 1/4 5%	R200,202,204,205, 207,307
14-5222/A	RES CF AX 2.2K 1/4W	R109,R119,120
14-5270/A	RES CF AX 27 1/4W 5%	R438
14-5274/A	RES CF 270K 1/4W 5%	R590,591
14-5302/A	RES CF 3K 5% 1/4W	R414,418,426

14-5362/A	RES CF AX 3.6K 1/4W 5%	R524,537
14-5392/A	RES CF AX 3.9K 1/4W 5%	R214
14-5470/A	RES CF AX 47 1/4W 5%	R308-311
14-5471/A	RES CF AX 470 1/4W 5%	R519,523,529,536
14-5472/A	RES CF AX 4.7K 1/4W 5%	R110,201,215-219,472
14-55R1/A	RES CF AX 5.1 1/4W 5%	R203
14-5513/A	RES CF AX 51K 1/4W 5%	531,539,471
14-5562/A	RES CF AX 5.6K 1/4W 5%	R469
14-5622/A	RES CF 6.2K 5% 1/4W	R415,419,428
14-5680/A	RES CF AX 68 1/4W 5%	R312-323,454,455, 457,458,460,461,462, 464,465,466
14-5750/A	RES CF 75 5% 1/4W	R407,409,410,420,425 427,432,434,R436,439
14-5821/A	RES CF 820 5% 1/4W	R467,468
C014179-05	CAP CER 47PF 50V 5%	C421
C014179-30	CAP CER 30PF 50V +-5% AX CH	C219,220,130
C014180-17	CAP CER .001UF 25V	C427,505,506,509, 510,517,518,521
C014180-18	CAP CER V.01UF 25V 20% AX	C503,515,101,540,527 533,549,430
C014180-25	CAP CER 8200PF 50V 20% AX	C528,531,534,538
C014181-05	CAP CER .22UF 50V -20+80% AX	C633-636
C014181-07	CAP CER .47UF 25V +80-20% AX	C411
C0770149-008	CAP CER 100PF 50V 5% SL AX	C222-225
C070290-001	CAP CER 150PF 50V 10% AX	C208
C070290-004	CAP CER 270PF 50V 10% AX	C218
C070290-005	CAP CER 330PF 50V 10% AX	C209
C070480-001	CAP CER .1UF 25V AX -20+80% Z	C104-106,108,109, 111-114,200,201,226 C300-307,402-406,409, 412-414,419,C500-502, 504,507,511-514,516,519, C523,524,632,206,203, 559,562,565,C207,210, 214,217,221,227-230, 422,C550-557,428,429, 900,536
C014384/A	IND FERRITE BEAD AD	L100,401,402,500-503

		410,508,510
C070471-002	IND 220UH 10% AX	L208
C101401-221	IND 220UF AX	L203

ASSY NO: SD400329-001

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
SA400429-001	ASSY SMD STE W/MOD	1
SB400329-101	ASSY SEQ STE NTSC W/MOD	1

ASSY NO: SA400329-001

PART NUMBER	DESCRIPTION	LOCATION/QUANTITY
C300779-001	PCB STE BLANK	1
C300589-001	IC STE MCU GLU 144P	U400

SECTION EIGHT:
GLOSSARY

1772 Floppy Disk Controller.

6850 Also ACIA (Asynchronous Communication Interface Adapter). Each one provides an asynchronous communications channel. In the STE, there are two 6850s, one for keyboard communication, and one for MIDI communication.

68901 See MFP.

BUS ERROR GSTMCU has asserted BERR to inform the processor that there is a problem with the current cycle. This could be due to a device not responding (for example, CPU tries to read memory but the Memory Controller fails to assert DTACK), or an illegal access (attempting to write to ROM). A bus error causes exception processing.

CPU The 68000 microprocessor.

DMA Direct Memory Access. Process in which data is transferred from external storage device to RAM, or from RAM to external storage. Transfer is very fast, and takes place independent of the CPU, so that the CPU can be processing while DMA is taking place. GSTMCU arbitrates the bus between the CPU and DMA.

DMA CONTROLLER Atari proprietary chip which controls the DMA process. All disk I/O goes through this device.

EXCEPTION A state in which the processor stops the current activity, saves what it will need to resume the activity later in RAM, fetches a vector (address) from RAM, and starts executing at the address vector. When the exception processing is done, the processor will continue what it was doing before the exception occurred. Exceptions can be caused by interrupts, instructions, or error conditions. See also System Errors, or a 68000 reference for more detail.

GSTMCU Atari proprietary chip which ties together all system timing and control signals.

HALT State in which the CPU is idle, all bus lines are in the high-impedence state, and can only be ended with a RESET input. This is a bidirectional pin on the CPU. It is driven externally by the RESET circuit on power-up or a reset button closure, and internally when a double bus fault occurs. A double bus fault is an error during a sequence which is run to handle a previous error. For example, if a bus error occurs, and during the exception processing for the bus error, another bus error occurs, then the CPU will assert HALT.

HSYNC Timing signal for the video display. Determines when horizontal scan is on the screen, and when it is blank (retracing). The synchronization (approx. every 63 microseconds) It is also encoded onto IPL2..0 to cause a level 2 auto-vectored interrupt to the CPU.

INTERRUPT A request by a device for the processor to stop what it is doing and perform processing for the device. It is a type of exception. Interrupts are maskable in software, meaning they will be ignored if they do not meet the current priority level of the CPU. There are three priorities:

The highest are MFP interrupts, then VSYNC interrupts, and lowest are HSYNC interrupts. Interrupts are signaled to the CPU on the Interrupt Priority Level inputs (IPL0-2). See Theory of Operation, Main System, MFP, and GSTMCU.

MEMORY CONTROLLER Atari proprietary chip which handles all RAM accesses. See Theory of Operation, Main System and Video Subsystem for details.

MIDI Musical Instrument Digital Interface. An electrical standard by which electronic instruments communicate. Also, the logical system for such communication. In the STE, consists of a 6850 communication chip, driver and receiver chips (74LS04, 74LS05, and PC-900 optoisolator), and an MFP interrupt channel.

MFP Multi-Function Peripheral, aka 68901. Interrupt control, timers, and USART for RS232 communication. See Theory of Operation, Main System.

MODULATOR Device which modulates a composite video signal, combined with audio, onto an RF carrier for output to a television.

PHASE LOCKED LOOP Circuit which locks the horizontal sync signal onto the color burst reference frequency for accurate color on the T.V. Without this circuit, colors on the T.V. become unstable, flickering or shifting about on the screen.

PSG Programmable Sound Generator, also YM2149. Yamaha version of General Instruments AY-3-8910. Has two 8 bit I/O ports and three sound channels. Used in parallel port and audio.

RS232C Electrical standard for serial digital communication. Also the physical and logical device which performs communication using this standard. In the STE computers, consists of the MFP, PSG, 1488, and 1489 chips.

SUPERVISOR MODE State of the CPU in which it is allowed to access all hardware and RAM locations, and perform some privileged instructions. Determined by the state of a bit in the Status Register.

USER MODE State of the CPU in which certain instructions and areas in the memory map are disallowed (resulting in a privilege violation exception if attempted). See also SUPERVISOR MODE.

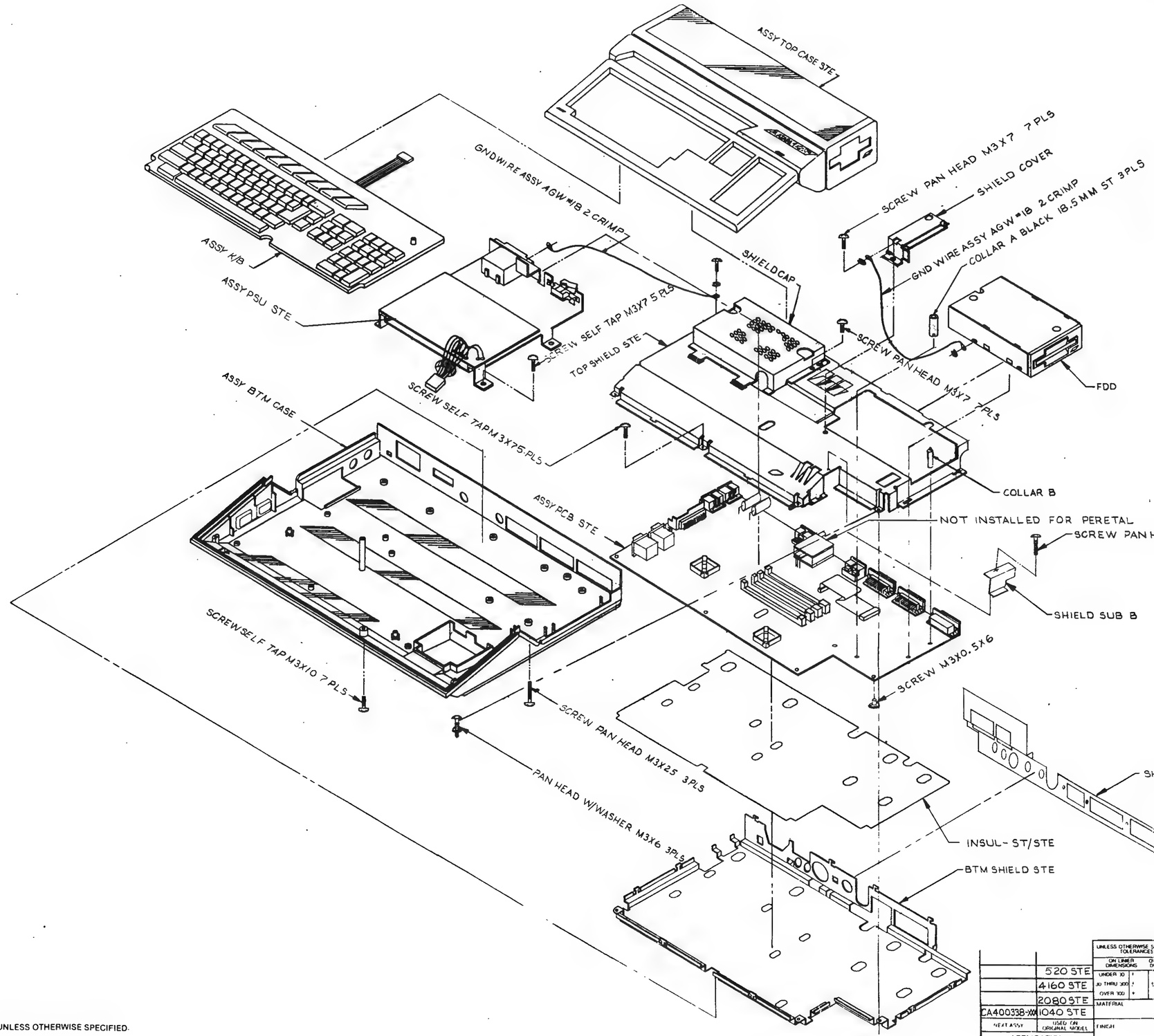
VSYNC Signal used for vertical synchronization of CRT display device. Occurs at 70 Hz (monochrome), or 50 or 60 HZ color.

YM2149 See PSG.

SECTION NINE:
SCHEMATICS AND SILKSCREENS

Assembly Drawing and Schematic Diagram

REV	REVISIONS DESCRIPTION	DATE	APPROVED
8	PRELIMINARY RELEASE	5-1-90	



NOTES—UNLESS OTHERWISE SPECIFIED.

	520 STE
	4160 STE
	2080 STE
CA400338-XX	1040 STE
NEXT ASSY	USED ON ORIGINAL MODEL
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES
ON LINEAR DIMENSIONS — UNDER 10 ±; 10 THRU 1000 ±; OVER 1000 ±
ON ANGULAR DIMENSIONS ±
MATERIAL
FINISH

DRAWN BY S. SURYSKA DATE 4-9-90
CHECKED DATE
ENGINEER DATE
APPROVED DATE
APPROVED DATE

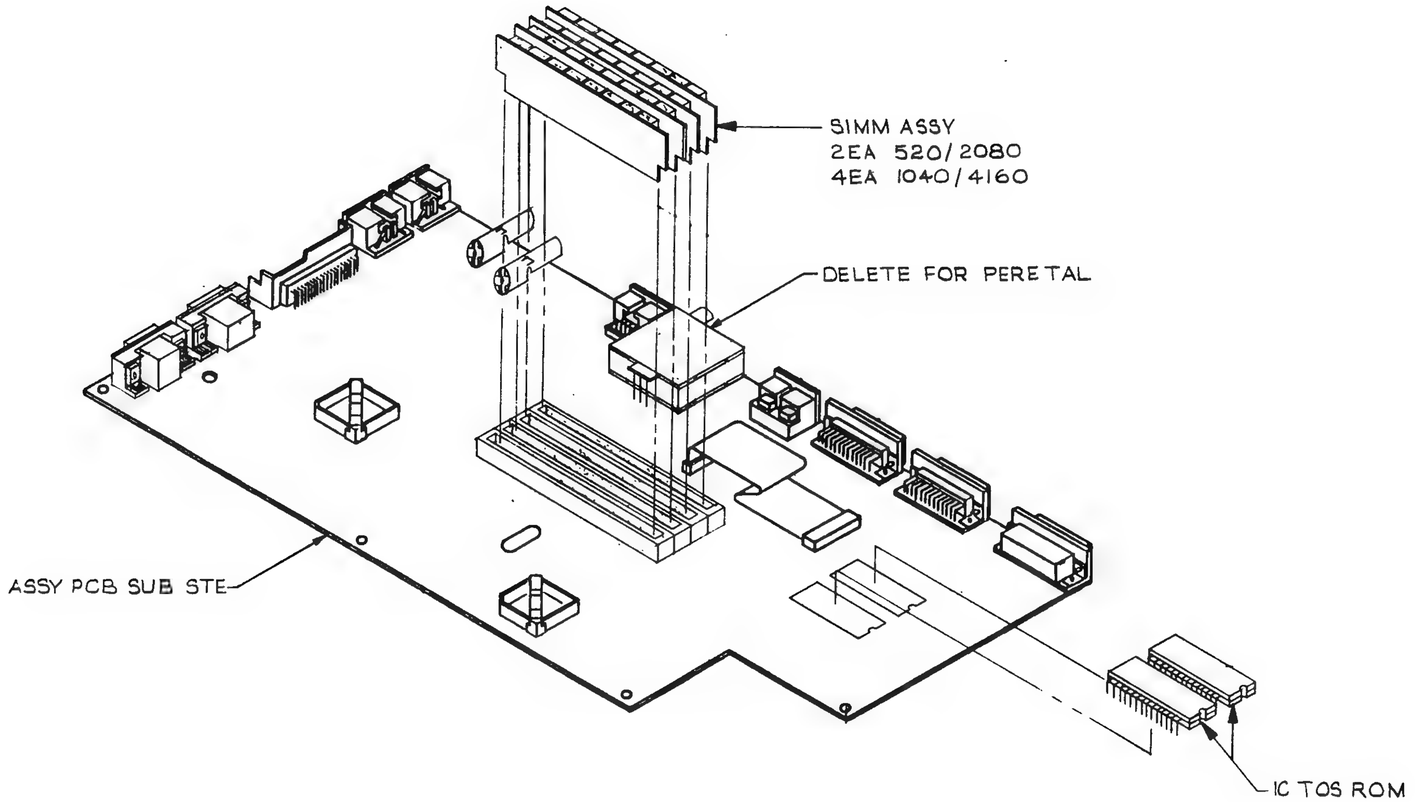
ATARI CORPORATION

TITLE ASSY MAIN

SIZE D | DRAWING NO CA4C0339-XXX | REV 8

SCALE | SHEET X OF 2

REV	REVISIONS DESCRIPTION	DATE	APPROVED
5	PRELIMINARY RELEASE	4/15/90	



NOTES—UNLESS OTHERWISE SPECIFIED:

	520 STE
	4160 STE
	2080 STE
CA400339-XXX	1040 STE
NEXT ASSY	USED ON ORIGINAL MODEL
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES	ON LINEAR DIMENSIONS	ON ANGULAR DIMENSIONS
UNDER 30	±	±
30 THRU 300	±	
OVER 300	±	
MATERIAL		
FINISH		

DRAWN BY / DATE	S. Simpson 4/11/90
CHECKED / DATE	
ENGINEER / DATE	
APPROVED / DATE	
APPROVED / DATE	

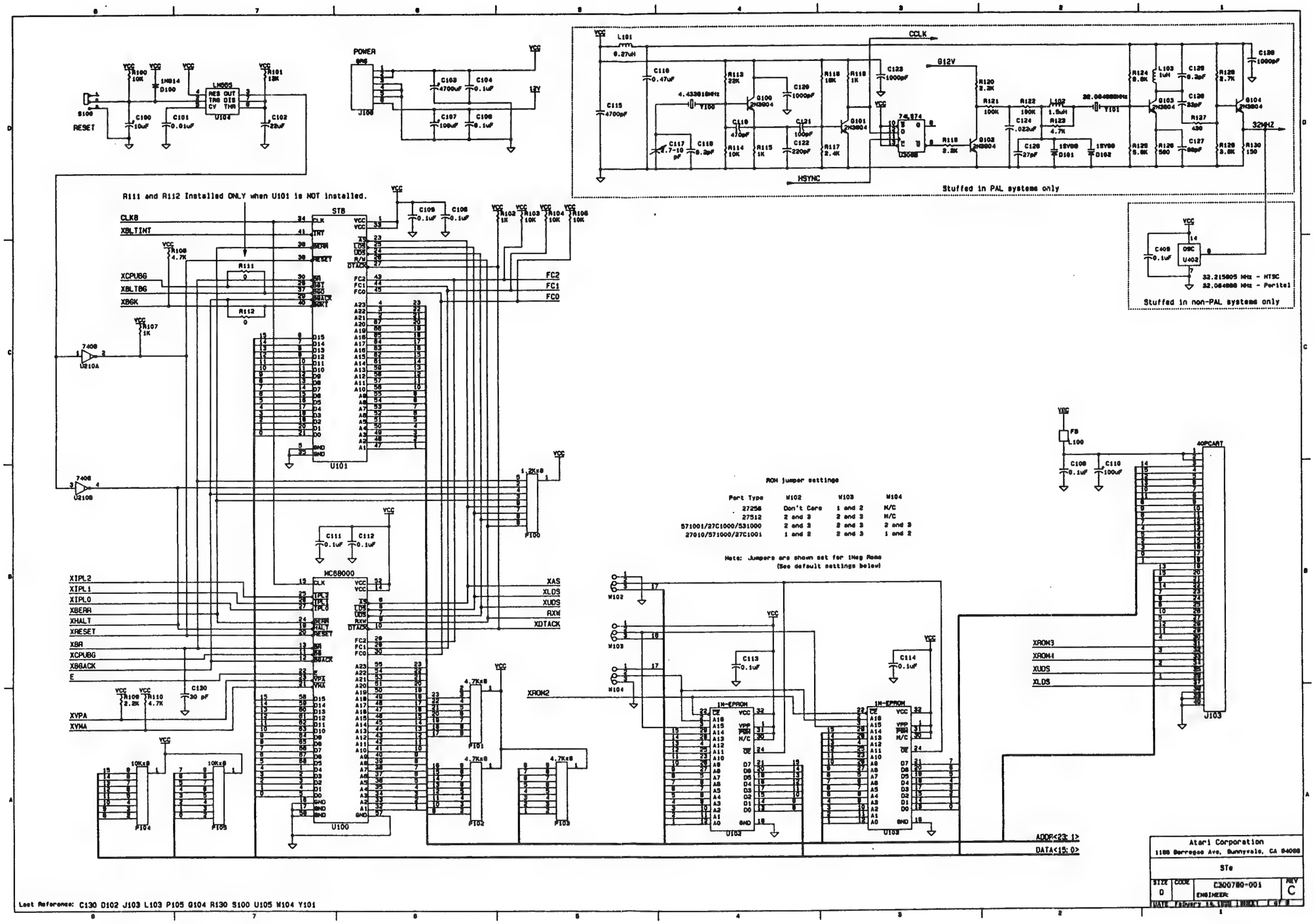
ATARI CORPORATION

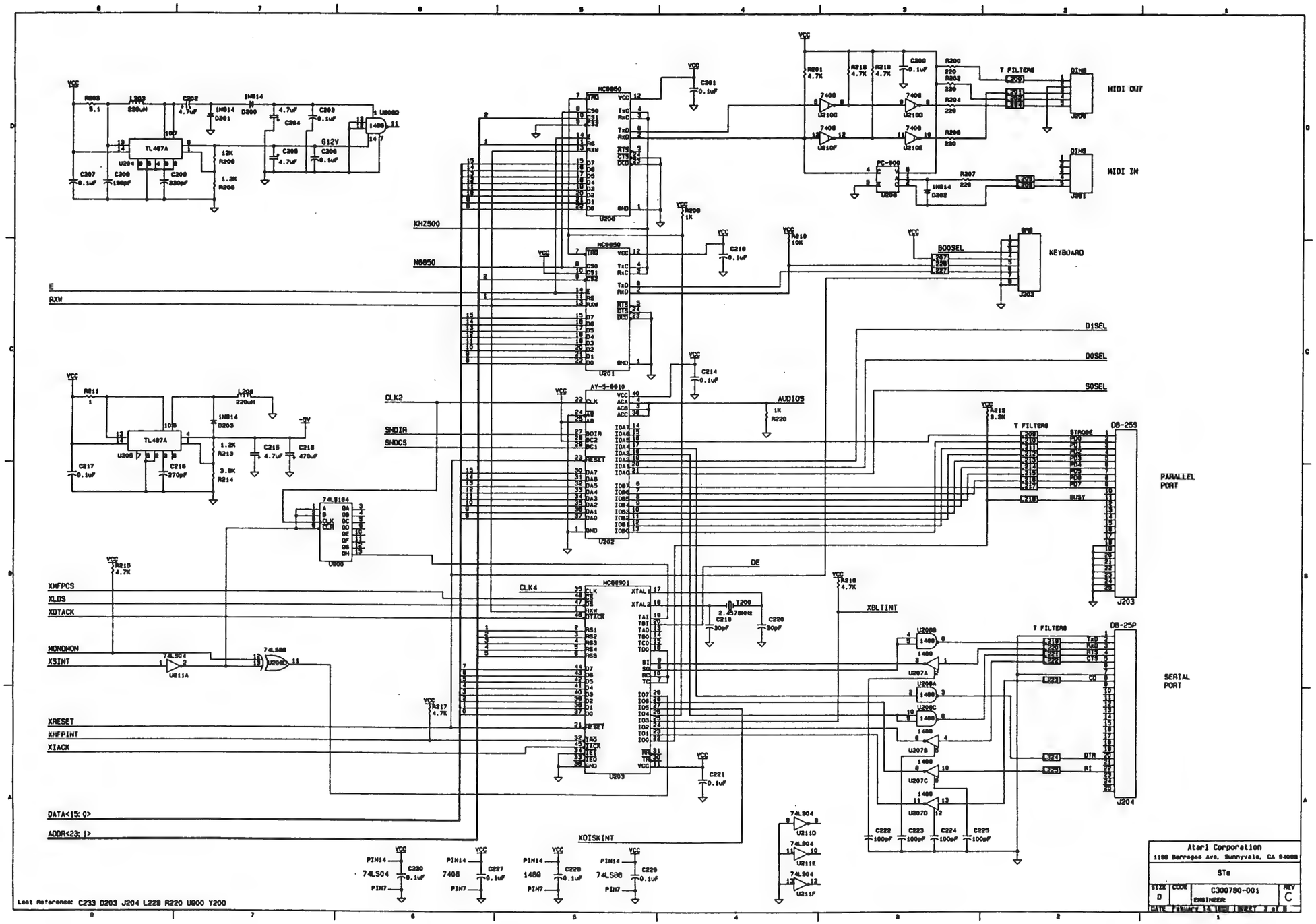
TITLE: ASSY PCB

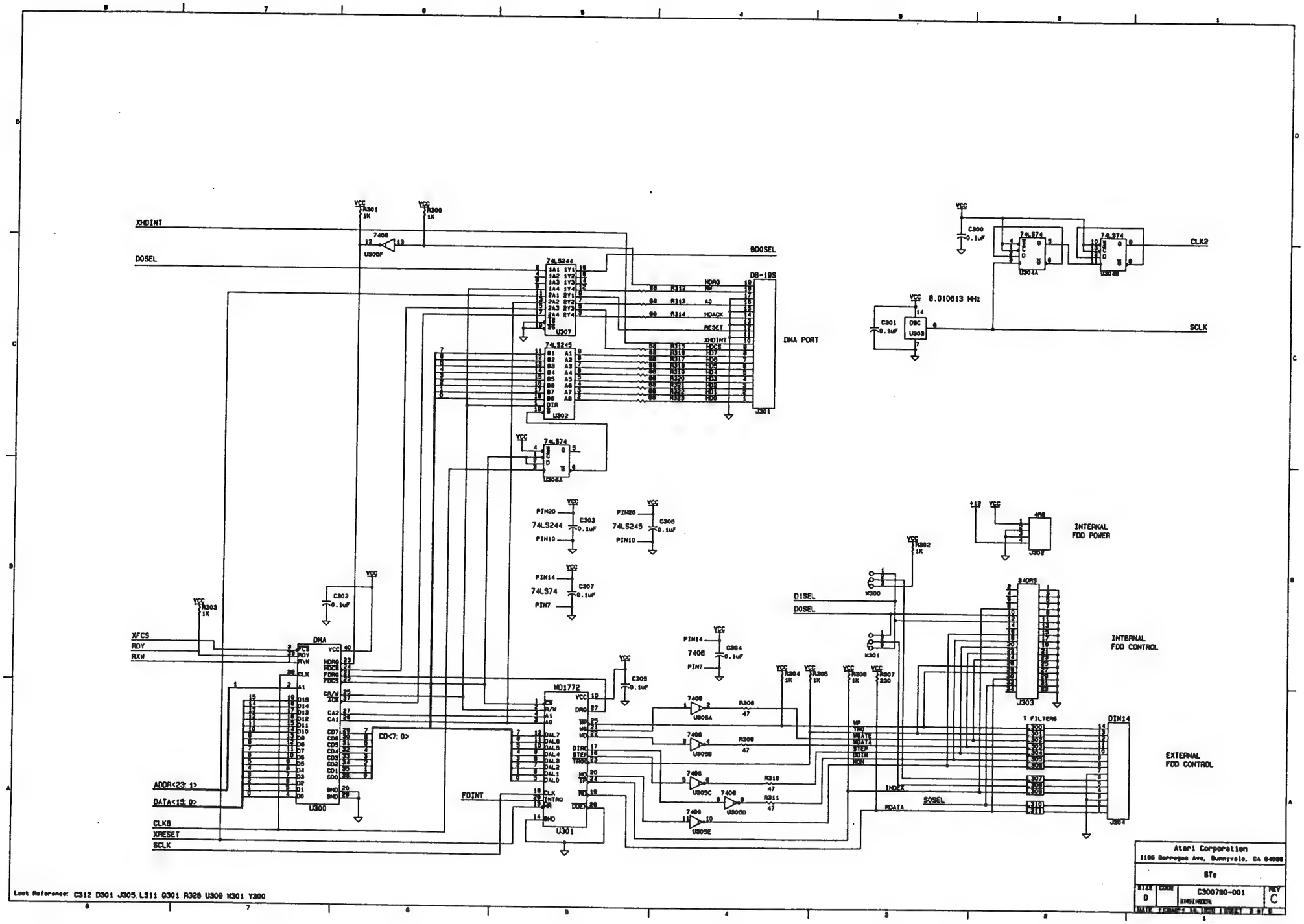
SIZE: C | DRAWING NO.: CA400340-XXX | REV: 5

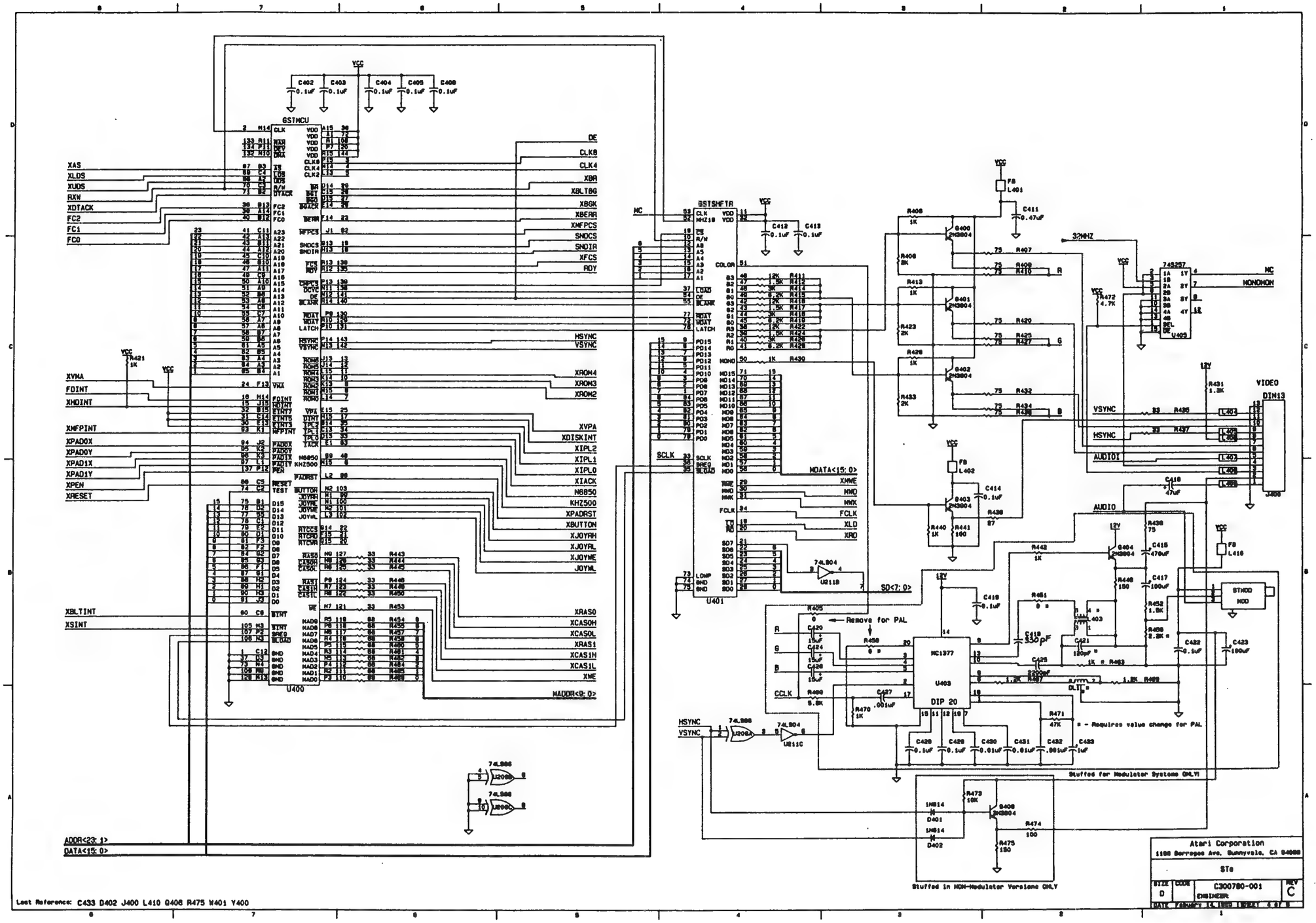
SCALE: ~ | SHEET X OF 3

THIRD ANGLE SYSTEM DIMENSION mm


R111 and R112 Installed ONLY when U101 is NOT installed.
RESET
POWER
CCLK
32MHZ
Stuffed in PAL systems only
Stuffed in non-PAL systems only
32.215905 MHz - NTSC
32.084988 MHz - Peritel
HSYNC
CLK8
XBLTINT
XCPUBG
XBLTBG
XBGK
STB
FC2
FC1
FC0
XAS
XLDS
XUDS
RXW
XDTACK
XIPL2
XIPL1
XIPL0
XBERR
XHALT
XRESET
XBR
XCPUBG
XBGACK
E
XVPA
XVMA
XROM2
XROM3
XROM4
ADDR<23:1>
DATA<15:0>
ROM jumper settings
Part Type W102 W103 W104
27256 Don't Care 1 and 2 N/C
27512 2 and 3 2 and 3 N/C
571001/27C1000/531000 2 and 3 2 and 3 2 and 3
27010/571000/27C1001 1 and 2 2 and 3 1 and 2
Note: Jumpers are shown set for 1Meg Roms
(See default settings below)
Atari Corporation
1196 Borregas Ave, Sunnyvale, CA 94088
STe
SIZE D
CODE
C300780-001
REV C
ENGINEER:
DATE February 14, 1990 SHEET 8 OF 8
Last Reference: C130 D102 J103 L103 P105 Q104 R130 S100 U105 W104 Y101


MIDI OUT
MIDI IN
KEYBOARD
PARALLEL PORT
SERIAL PORT
KHZ500
N6850
CLK2
SNDIA
SNDCS
AUDIOS
DISEL
DOSEL
SOSEL
BOOSEL
DE
XBLTINT
XDISKINT
XMFPCS
XLDS
XDTACK
MONOMON
XSINT
XRESET
XMFPINT
XIACK
DATA<15:0>
ADDR<23:1>
CLK4
Last Reference: C233 D203 J204 L228 R220 U900 Y200
Atari Corporation
1196 Borregas Ave. Sunnyvale, CA 94088
STe
C300780-001
ENGINEER:
SIZE D
REV C


XHDINT
DOSEL
BOOSEL
DB-19S
DMA PORT
74LS244
74LS245
U307
U302
U306A
U306B
U306C
U306D
U306E
U306F
U300
U301
WD1772
DMA
XFCS
RDY
R/W
A0
CD<7:0>
ADDR<23:1>
DATA<15:0>
CLK8
XRESET
SCLK
FDINT
HDRQ
HDACK
RESET
C300
C301
C302
C303
C304
C305
C306
C307
0.1uF
8.010613 MHz
OSC
U303
74LS74
U304A
U304B
CLK2
SCLK
INTERNAL
FDD POWER
J302
INTERNAL
FDD CONTROL
J303
EXTERNAL
FDD CONTROL
J304
DISEL
SOSEL
INDEX
RDATA
T FILTER8
DIN14
R300
R301
R302
R303
R304
R305
R306
R307
R308
R309
R310
R311
R312
R313
R314
R315
R316
R317
R318
R319
R320
R321
R322
R323
1K
220
47
Last Reference: C312 D301 J305 L311 Q301 R328 U309 W301 Y300
Atari Corporation
1196 Borregas Ave. Sunnyvale, CA 94088
STe
SIZE D
CODE
C300780-001
REV C
ENGINEER:
DATE


GSTMCU
U400
GSTSHFTR
U401
XAS
XLOS
XUDS
RXW
XDTACK
FC2
FC1
FC0
XVMA
FDINT
XHDINT
XMFPINT
XPAD0X
XPAD0Y
XPAD1X
XPAD1Y
XPEN
XRESET
XBLTINT
XSINT
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DATA<15:0>
DE
CLK8
CLK4
XBR
XBLTBG
XBGK
XBERR
XMFPCS
SNDCS
SNDIR
XFCS
RDY
HSYNC
VSYNC
XROM4
XROM3
XROM2
XVPA
XDISKINT
XIPL2
XIPL1
XIPL0
XIACK
N6850
KHZ500
XPADRST
XBUTTON
XJOYFH
XJOYFL
XJOYME
JOYML
XRAS0
XCAS0H
XCAS0L
XRAS1
XCAS1H
XCAS1L
XME
MADDR<9:0>
MDATA<15:0>
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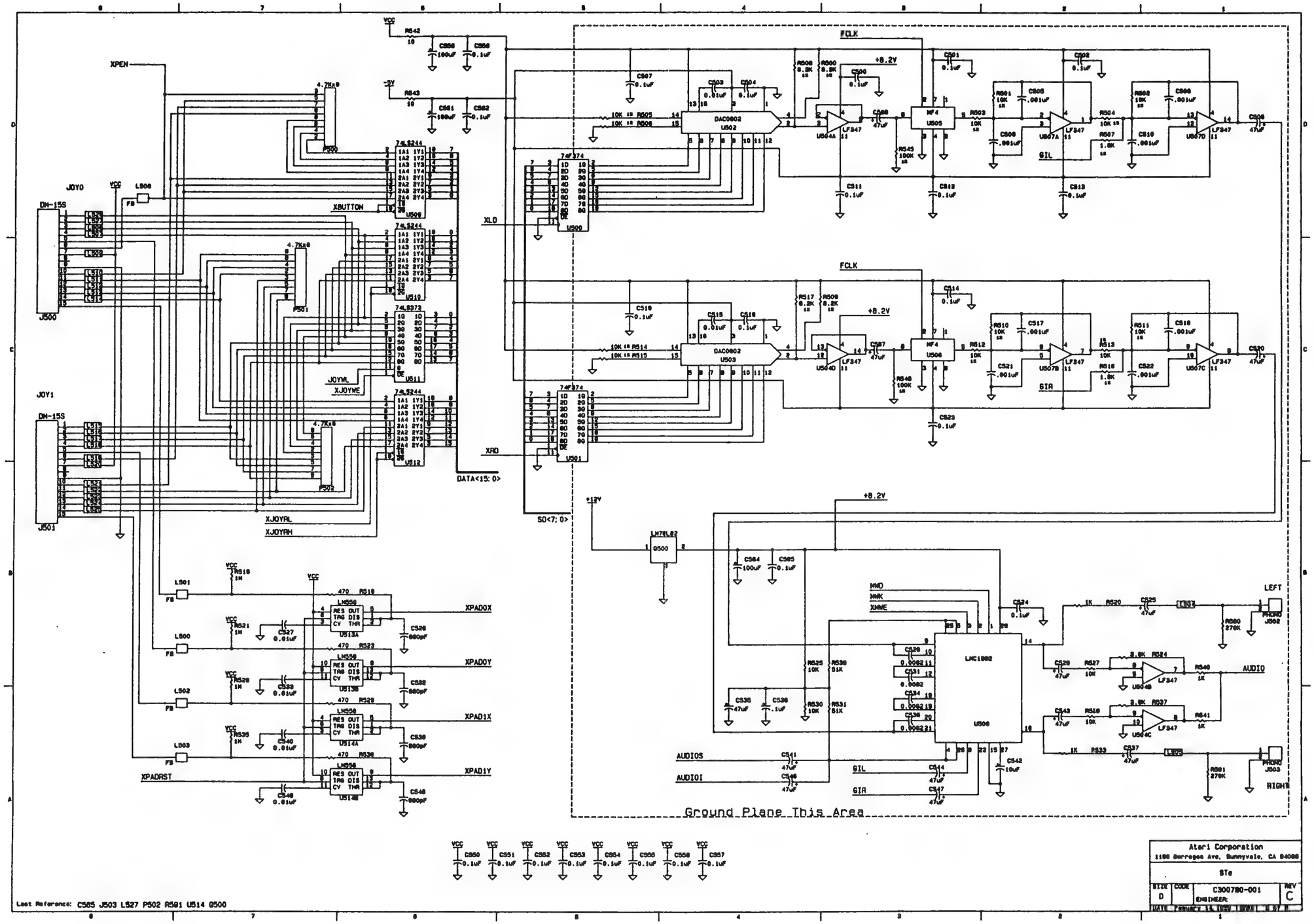
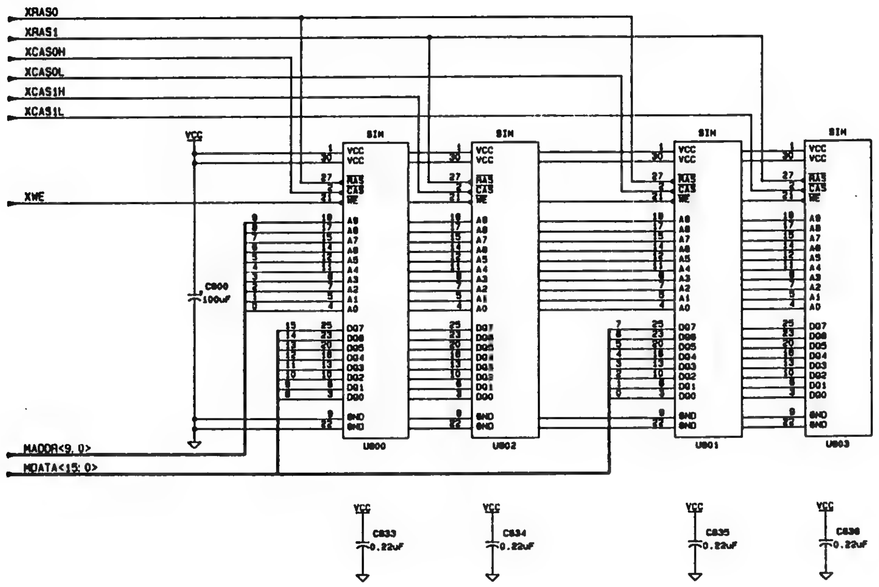
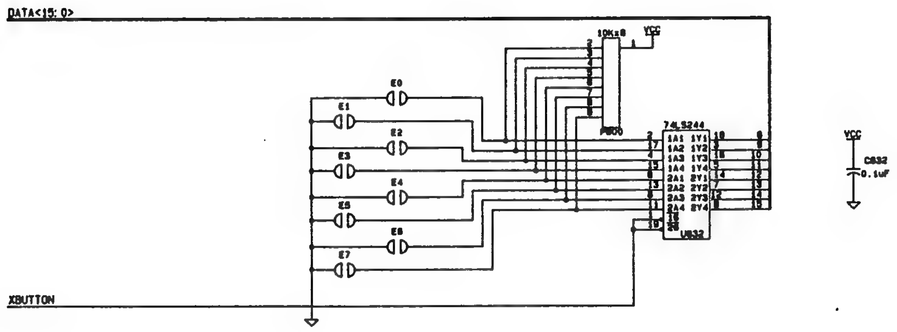
XWO
WMK
FCLK
XLO
XRO
SD<7:0>
SCLK
LOAD
BLANK
COLOR
MC
32MHZ
MONOMON
VIDEO
DIN13
AUDIO
AUDIO1
Remove for PAL
MC1377
DIP 20
Stuffed for Modulator Systems ONLY
Stuffed in NON-Modulator Versions ONLY
Atari Corporation
1196 Borregas Ave. Sunnyvale, CA 94088
STe
C300780-001
REV C
Last Reference: C433 D402 J400 L410 Q406 R475 W401 Y400


XPEN
JOY0
DH-15S
J500
JOY1
DH-15S
J501
VCC
-5V
+12V
+8.2V
FCLK
XBUTTON
JOYWL
XJOYWE
XJOYRL
XJOYRH
DATA<15:0>
XLD
XRD
SD<7:0>
XPADRST
XPADOX
XPADOY
XPAD1X
XPAD1Y
AUDIOS
AUDIOI
GIL
GIR
MWD
MWK
XHWE
LEFT
RIGHT
AUDIO
Ground Plane This Area
Atari Corporation
1196 Borregas Ave, Sunnyvale, CA 94088
STe
C300780-001
Last Reference: C585 J503 L527 P502 R591 U514 Q500

REV	REVISIONS DESCRIPTION	DATE	APPROVED
B	PRODUCTION RELEASE		
C	REVISED PER ECR AS-0173		





Last Reference: C836 J800 P800 R802 U832 W807

NEXT ASSY	USED ON ORIGINAL MODEL
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES		
ON LINER DIMENSIONS	ON ANGULAR DIMENSIONS	
UNDER 30 ±	±	
30 THRU 300 ±		
OVER 300 ±		
MATERIAL		
FINISH		

DRAWN BY	DATE
CHECKED	DATE
ENGINEER	DATE
APPROVED	DATE
APPROVED	DATE

ATARI CORPORATION

TITLE: SCHEMATIC DIAGRAM STE

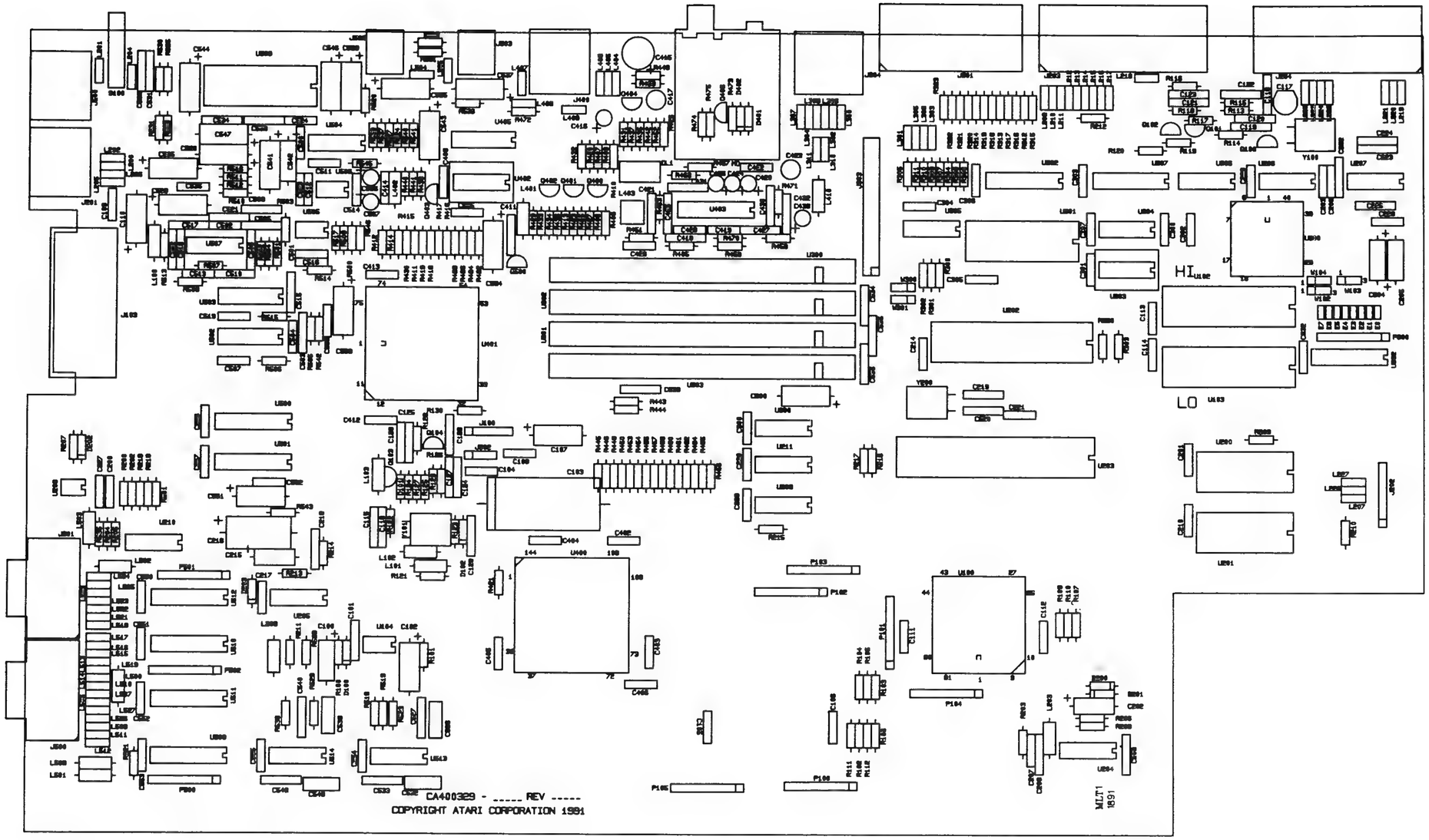
SIZE	DRAWING NO.	REV
C	C300780-001	C

SCALE —————— SHEET 6 OF 6

THIRD ANGLE SYSTEM DIMENSION . mm

129287

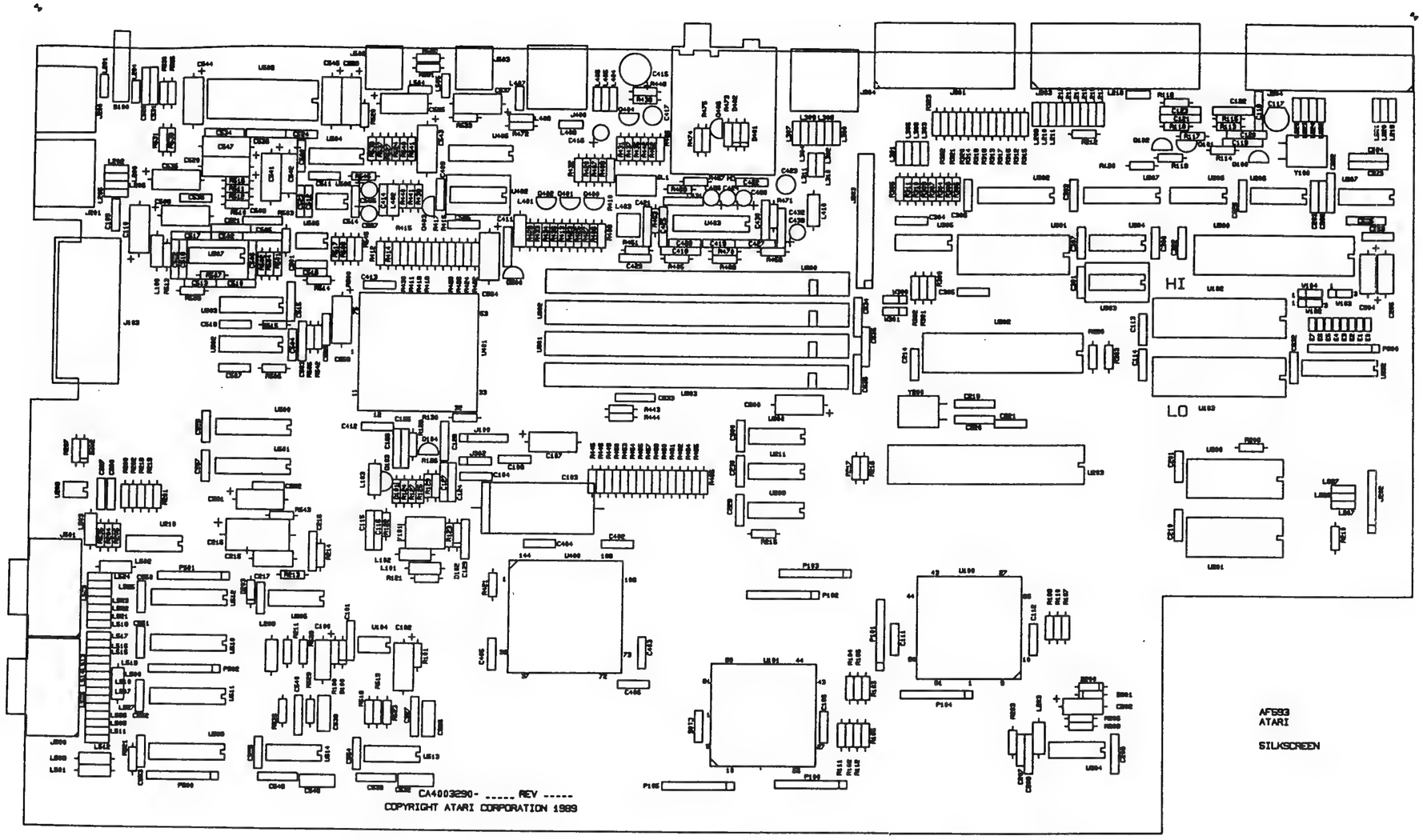
PCB Silk Screen



ATARI
4115 KELLER SPRINGS ROAD SUITE 200
DALLAS, TEXAS 75244

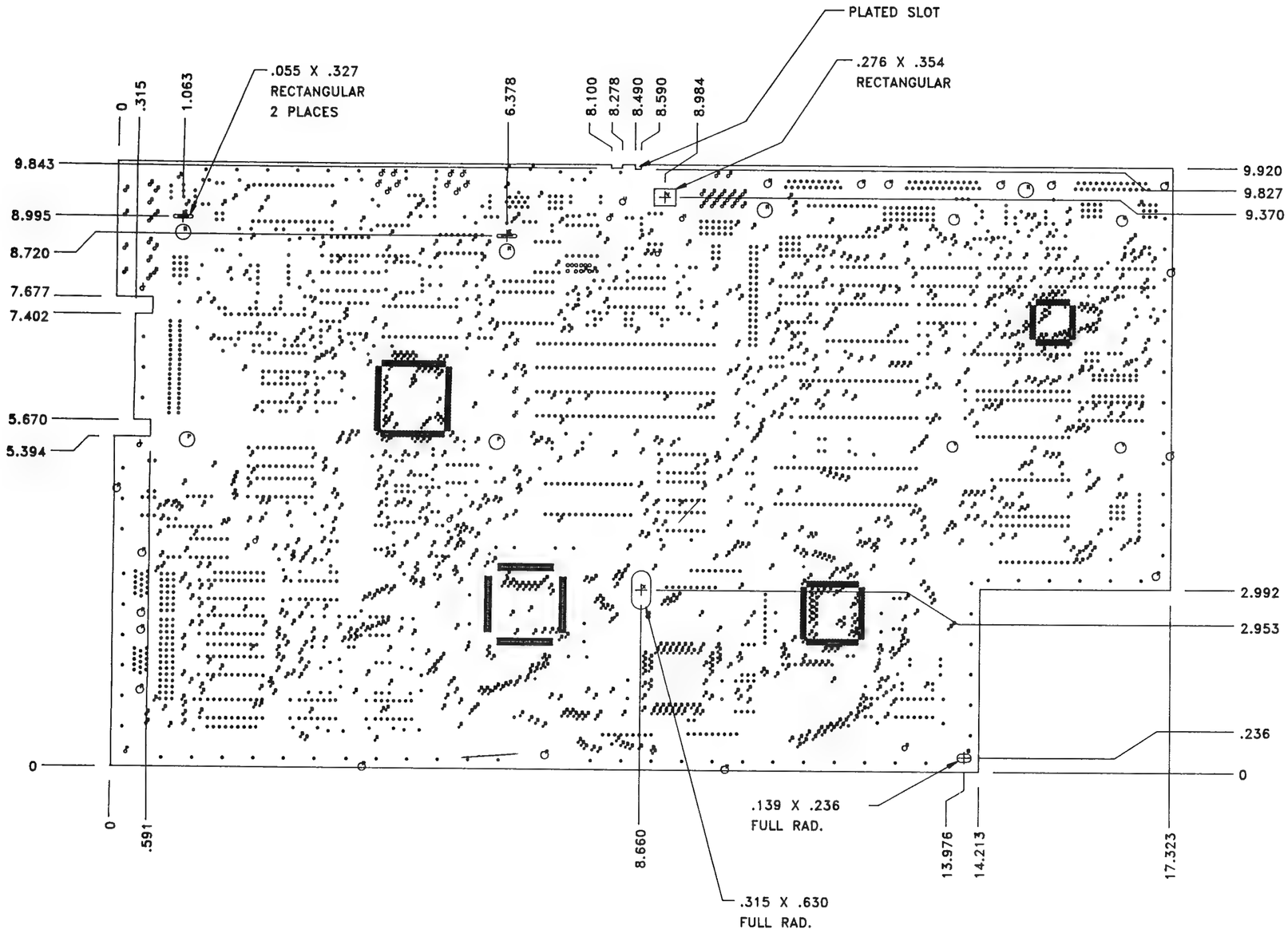
STE
C300779-001
REV C

LAYER SS
SILKSCREEN


HI
LO
AF693
ATARI
SILKSCREEN
CA4003290- ----- REV -----
COPYRIGHT ATARI CORPORATION 1989

PCB Component Side

REV	REVISION DESCRIPTION	DATE	APPROVED
C	REVISED PER ECO #[redacted] 1314	5/17/91	TJH

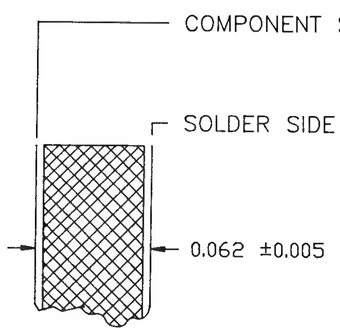


NOTES: UNLESS OTHERWISE SPECIFIED

1. MATERIAL: BASE MATERIAL LAMINATED EPOXY GLASS GRADE NEMA FR-4, 1 .OZ COPPER PER MIL P-13949 AND UL APPROVED MANUFACTURED SOURCE.
2. SOLDERMASK BOTH SIDES, WET PHOTO IMAGABLE OR DRY FILM COLOR GREEN.
3. ALL HOLES SHALL BE LOCATED WITHIN .005 ANNULAR RING OF TRUE POSITION OF LOCATION SHOWN ON MASTER PATTERN.
4. SILKSCREEN COMP SIDE, COLOR WHITE, SILKSCREEN SOLDER SIDE, COLOR WHITE.
5. WARP OR TWIST OF COMPLETED PCB NOT TO EXCEED .007 IN/IN.
6. PLACE VENDOR LOGO AND DATE CODE ON SOLDER SIDE.
7. FINISH: SOLDERMASK OVER BARE COPPER (SMOBC), TRACE REDUCTION/EXPANSION SHALL NOT EXCEED ±20%.

HOLE CHART

CODE	SIZE ±.003	DESCRIPTION	QTY
—	.038	PLATED THRU	2245
B	.028	PLATED THRU	1057
D	.050	PLATED THRU	43
E	.055 X .327	PLATED THRU	2
F	.068	PLATED THRU	4
G	.075	PLATED THRU	30
H	.090	PLATED THRU	2
K	.097	PLATED THRU	12
L	.118	PLATED THRU	2
M	.125	PLATED THRU	8
P	.138	PLATED THRU	14
Q	.139 X .236	NOT PLATED	1
R	.150	NOT PLATED	4
S	.165	NOT PLATED	1
U	.237	PLATED THRU	2
V	.276	PLATED THRU	3
W	.276 X .354	NOT PLATED	1
X	.315 X .630	NOT PLATED	1



SILKSCREEN ONE SIDE (1 FILM)	YES	VOLTAGE	NO		
		GROUND	NO		
COMP SIDE	YES	SOLDERMASK BOTH SIDES (2 FILMS)	YES	CA400329	STE
SOLDER SIDE	YES			NEXT ASSY	USED ON ORIGINAL MODEL
PADMASTER	YES				
FILM REQUIRED				APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON LINED DIMENSIONS / ON ANNULAR DIMENSIONS
.XX ±0.01
.XXX ±0.005
±2°
MATERIAL [1]
FINISH

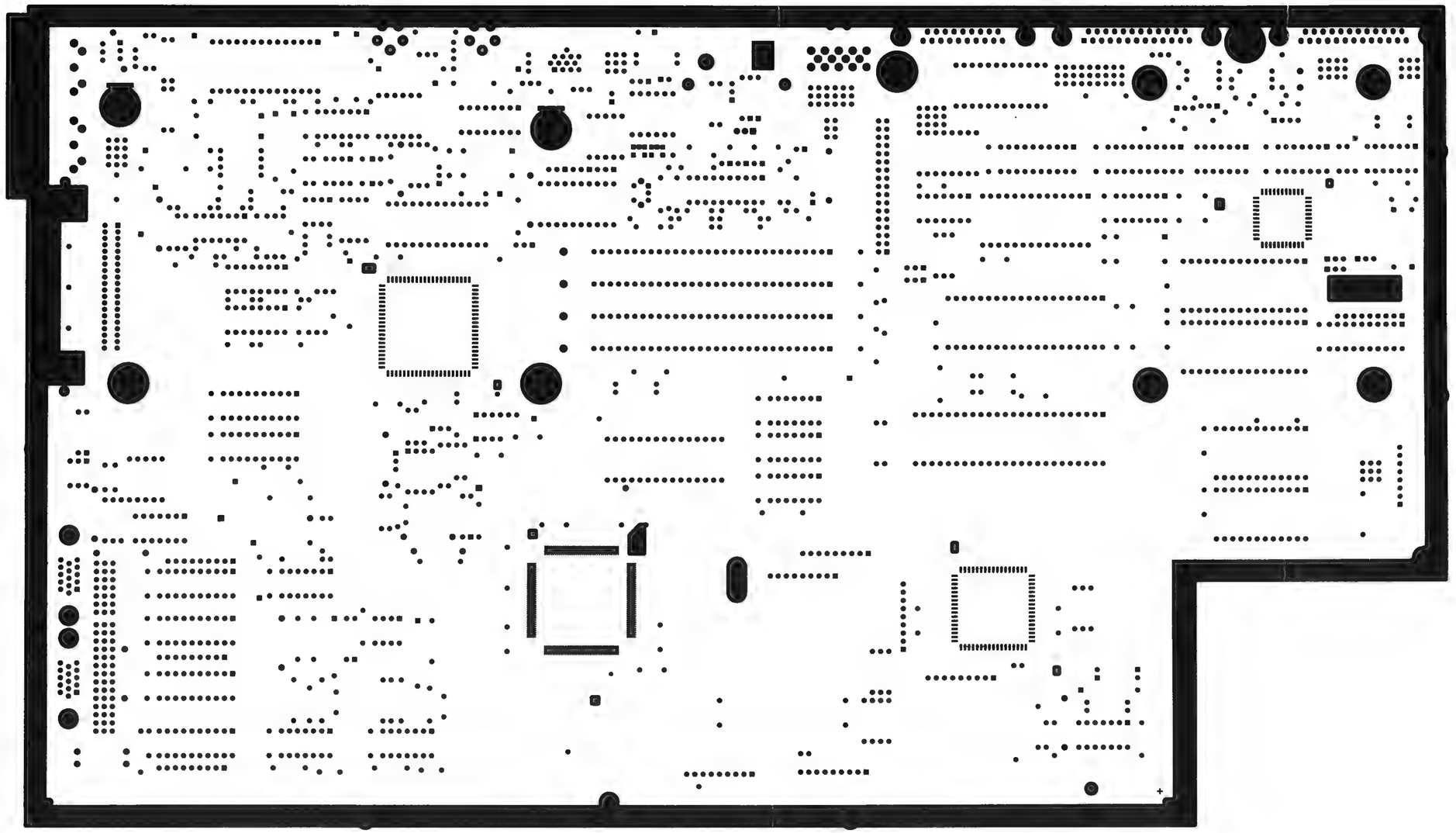
DRAWN BY: DATE:
CHECKED: DATE:
ENGINEER: DATE:
APPROVED: DATE: TJH 5/17/91
APPROVED: DATE:

ATARI MICROSYSTEMS CORPORATION
4115 KELLER SPRING RD., SUITE 200
DALLAS, TEXAS 75244

TITLE: FAB DRAWING, STE

SIZE A1 | DRAWING NO. C300779 | REV C

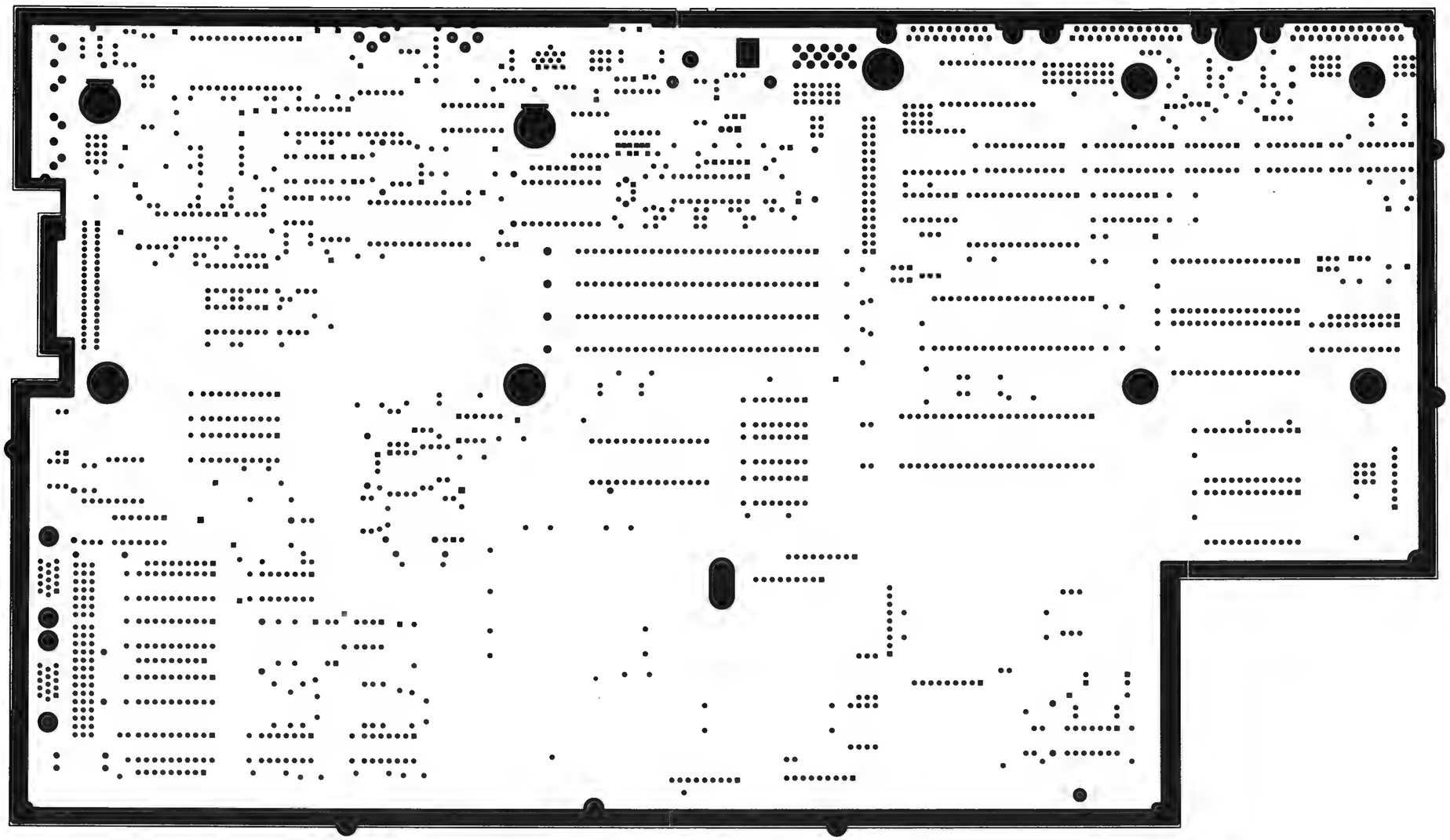
SCALE NONE | SHEET 1 OF 1



ATARI
4115 KELLER SPRINGS ROAD SUITE 200
DALLAS, TEXAS 75244

STE
C300779-001
REV C

LAYER SM1
COMPONENT SIDE SOLDERMASK



ATARI
4115 KELLER SPRINGS ROAD SUITE 200
DALLAS, TEXAS 75244

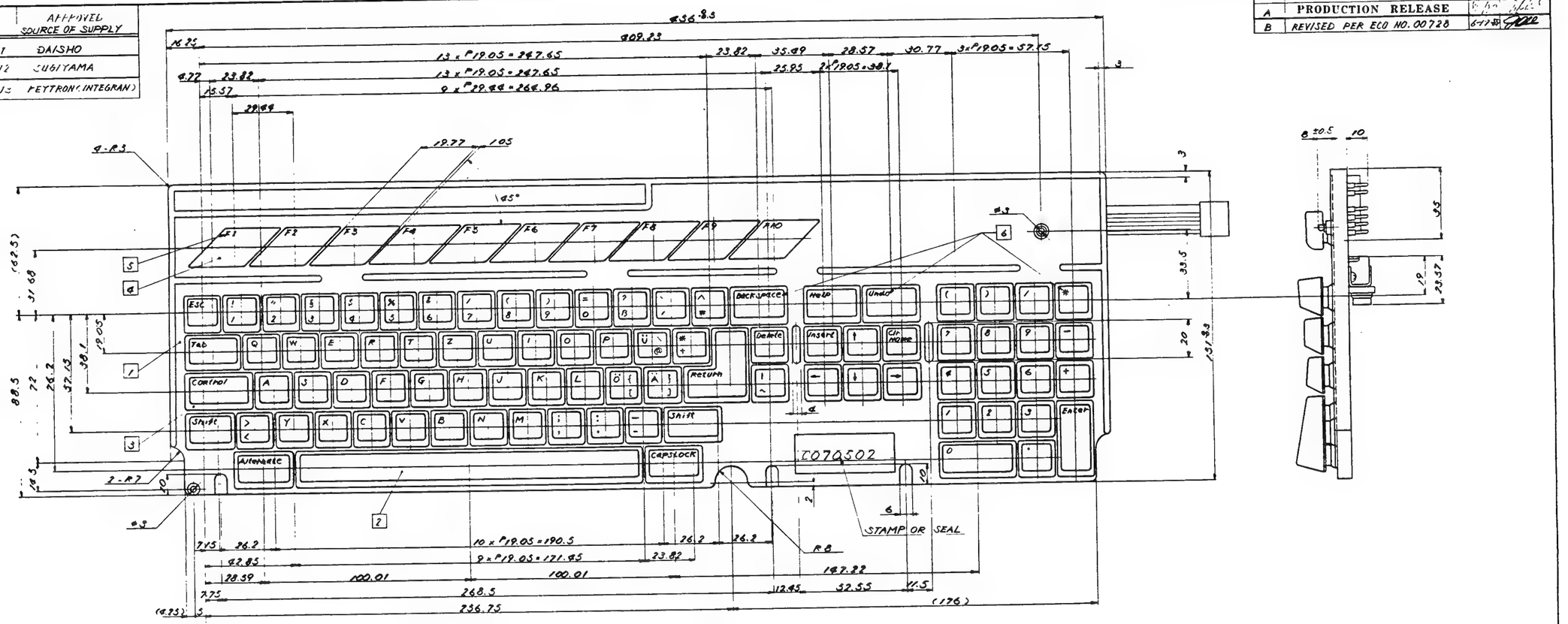
STE
C300779-001
REV C

LAYER SM2
SOLDERMASK SOLDER SIDE

Keyboards, US and European

PART NO.	APPROVED SOURCE OF SUPPLY
C070502-011	DAISHO
-012	SUGIYAMA
C070502-013	KEYTRON(INTEGRAN)

REV	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	6.10.88	
B	REVISED PER ECO NO. 00728	6.17.88	



CONNECTOR ASSIGNENT

PIN NO	NAME	WIRE COLOR
1	GND	YELLOW
2	KEY (NC)	
3	DRIVE 0 SELLECT	BLACK
4	VCC → 5V	
5	TX DATA	
6	RX DATA	
7	REJET	
8	GND	BLACK

3. FUNCTIONKEY : KEYCAP SURFACE TEXTURE NO.114 (FUJITA KOGYO)
2. ALPHA NUMERIC KEY
: KEYCAP TOP SURFACE TEXTURE NO.117 (FUJITA KOGYO)
: KEYCAP FRONT SURFACE TEXTURE NO MVF100 (FUJITA KOGYO)

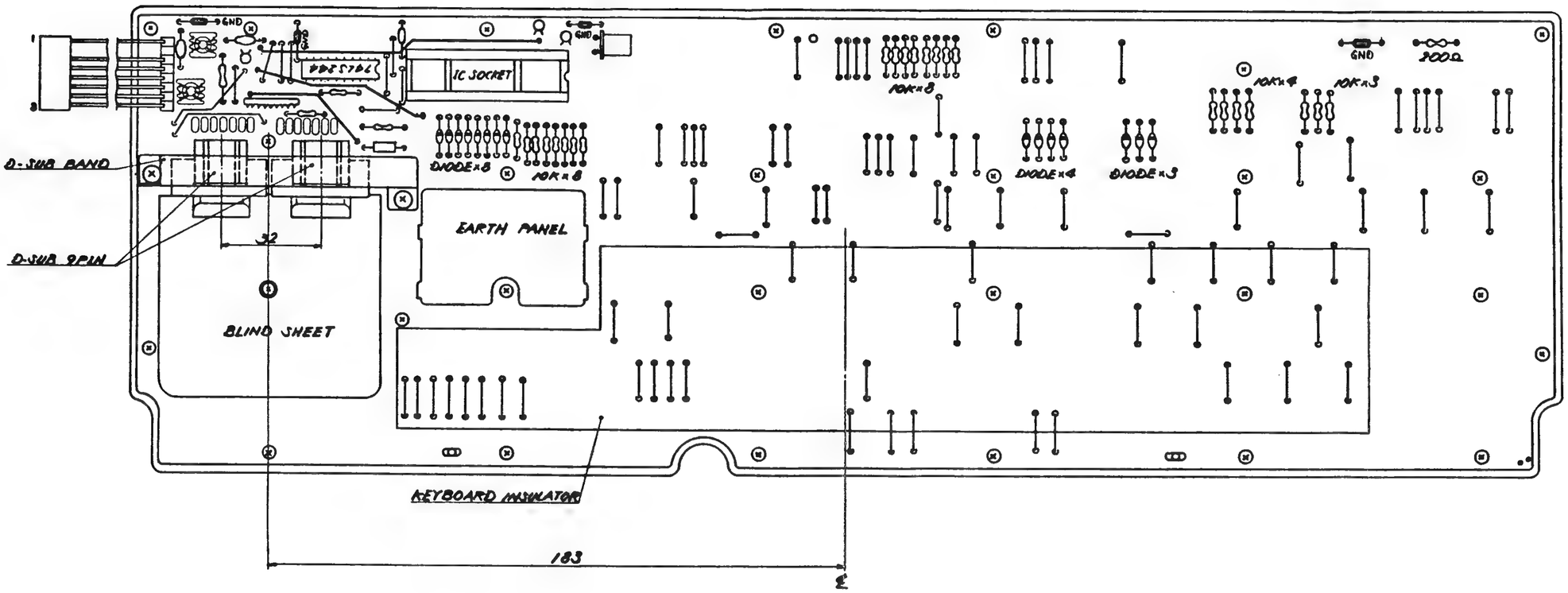
6	ABS	C100142-001	ATARI LIGHT BROWN
5		-001	ATARI IVORY
4		-001	ATARI LIGHT GRAY I
3		-001	ATARI IVORY
2		-001	ATARI IVORY
1	ABS	C100142-001	ATARI IVORY
	MATERIAL	COLOR NO.	COLOR DESCRIPTION

1.

NOTES-UNLESS OTHERWISE SPECIFIED:

EDITION: V2.05TFM	DRAWN BY / DATE: [illegible] 12.28.88	ATARI (JAPAN) CORPORATION Toranomon Kyoshi Building 3F 4-3-10. Toranomon Minato-ku Tokyo 105
NEXT ASSY: CA070057-XXX	CHECKED / DATE: [illegible]	
MATERIAL:	ENGINEER / DATE: [illegible]	TITLE: KEYBOARD 95KEY (GERMANY)
FINISH:	APPROVED / DATE: [illegible]	SIZE: C DRAWING NO: C070502 REV: E
	APPROVED / DATE: [illegible]	SCALE: NONE SHEET 1 OF 3

REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON	DRAWN BY / DATE	ATARI (JAPAN) CORPORATION	
NEXT ASSY	CHECKED / DATE 12-25-86	Toranomon Kiyoshi Building 3F	
MATERIAL	ENGINEER / DATE 12-24-86	4-3-10, Toranomon Minato-ku, Tokyo 105	
FINISH	APPROVED / DATE	TITLE: KEYBOARD 95KEY (GERMANY)	
	APPROVED / DATE 1/5/87	SIZE C · DRAWING NO. C070502 · REV B	
		SCALE 1/1 · SHEET 2 OF 3	

ASSY NO.	DESCRIPTION
CA070057-001	ENG (USA) - CANADA
-002	ENG (UK)
-003	GERMAN (NON-FTZ)
-004	FRENCH
-005	ENG(USA) - USA
-006	GERMAN (FTZ)
-007	SPANISH
-008	SWEDISH
-009	TURKISH
-010	SWISS - FRENCH
-011	SWISS - GERMAN
-012	NORWEGIAN
-013	ARABIC
-014	ITALIAN
CA070057-015	SWISS

REV.	REVISIONS DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	11/2/85	
B	REVISED PER ECO. NO. 00178	12-12-85	
C	REVISED PER ECO NO. 00206	2/17/86	
D	REVISED PER ECO NO. 00275	6-24-86	
E	REVISED PER ECO NO. 00671	5-13-88	
F	REVISED PER ECO NO. 00764	7-26-88	
G	REVISED PER ECO NO. 01103	4/28/89	

NOTES-UNLESS OTHERWISE SPECIFIED :

USED ON: 1040STF (KEYBOARD)	DRAWN BY / DATE: C. Ueda 8-22-85	ATARI (JAPAN) CORPORATION Toranomon Kiyoshi Building 3F 4-3-10, Toranomon Minato-ku, Tokyo 105
NEXT ASSY: CA070054-XXX, CA070074-XXX	CHECKED / DATE: K. Kitagawa 9-20-85	TITLE: ASSY KEYBOARD 1040STF (K/B)
MATERIAL	ENGINEER / DATE: 9 20.85	SIZE B · DRAWING NO CA070057-XXX · REV G
FINISH	APPROVED / DATE: 7/12/88	SCALE NONE · SHEET 1 OF 4
	APPROVED / DATE: 9/25/85	

THIRD ANGLE SYSTEM DIMENSION mm

A/N: CA070057-xxx	REV. G	TITLE: ASSY KEYBOARD 1040STF (K/B)	MODEL: 1040STF (KEYBOARD)

REV	REVISION DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		

ATARI

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

VERSION	STANDARD	MARKET
	SEE SHEET 1.	

A/N: CA070057-XXX

SHEET 2 OF 4

ITEM NO.	PART NUMBER	DESCRIPTION	QTY. REQUIRED PER VERSION											
			-001	-002	-003	-004	-005	-006	-007	-008	-009	-010	-011	-012
1														
2														
3	C0703004	KEYBOARD (CAN)	ALT	–	–	–	–	–	–	–	–	–	–	–
4	C0703005	(GERMANY)	–	–	1	–	–	–	–	–	–	–	–	–
5	C0703006	(FRANCE)	–	–	–	ALT	–	–	–	–	–	–	–	–
6	C0703007	(UK)	–	ALT	–	–	–	–	–	–	–	–	–	–
7	C0705001	(USA)	–	–	–	–	ALT	–	–	–	–	–	–	–
8	C0705002	(GERMANY)	–	–	–	–	–	ALT	–	–	–	–	–	–
9	C070597	KEYBOARD (USA)	–	–	–	–	ALT	–	–	–	–	–	–	–
10														
11														
12														
13														
14														
15														
16														
17	C0701122-002	IC, 6301V1. 1CHIP CPU VER 63V2.0	1	1	1	1	1	1	1	1	1	1	1	1
18														
19														
20														
21	CA070138-001	ASSY KEYBOARD CONSOLE USA 94KEY	–	–	–	–	1	–	–	–	–	–	–	–
22	-002	GERMANY 95KEY	–	–	–	–	–	1	–	–	–	–	–	–
23	-003	UK 95KEY	–	1	–	–	–	–	–	–	–	–	–	–
24	-004	FRANCE 95KEY	–	–	–	1	–	–	–	–	–	–	–	–
25	-005	CANADA 94KEY	1	–	–	–	–	–	–	–	–	–	–	–
26	-006	SPAIN 95KEY	–	–	–	–	–	–	1	–	–	–	–	–
27	-007	SWEDEN 95KEY	–	–	–	–	–	–	–	1	–	–	–	–
28	-008	TURKISH 95KEY	–	–	–	–	–	–	–	–	1	–	–	–
29	-009	SWISS-FRENCH 95KEY	–	–	–	–	–	–	–	–	–	1	–	–
30	-010	SWISS-GERMAN 95KEY	–	–	–	–	–	–	–	–	–	–	1	–
31	CA070138-011	ASSY KEYBOARD CONSOLE NORWEGIAN 95KEY	–	–	–	–	–	–	–	–	–	–	–	1
32														
33														
34	CA200432-001	ASSY KEYBOARD CONSOLE USA 94KEY	–	–	–	–	ALT	–	–	–	–	–	–	–
35	-002	GERMANY 95KEY	–	–	–	–	–	ALT	–	–	–	–	–	–
36	-003	UK 95KEY	–	ALT	–	–	–	–	–	–	–	–	–	–
37	-004	FRANCE 95KEY	–	–	–	ALT	–	–	–	–	–	–	–	–
38	-005	CANADA 94KEY	ALT	–	–	–	–	–	–	–	–	–	–	–
39	-006	SPAIN 95KEY	–	–	–	–	–	–	ALT	–	–	–	–	–
40	-007	SWEDEN 95KEY	–	–	–	–	–	–	–	ALT	–	–	–	–
41	-008	TURKISH 95KEY	–	–	–	–	–	–	–	–	ALT	–	–	–
42	-009	SWISS-FRENCH 95KEY	–	–	–	–	–	–	–	–	–	ALT	–	–
43	-010	SWISS-GERMANY 95KEY	–	–	–	–	–	–	–	–	–	–	ALT	–
44	CA200432-011	ASSY KEYBOARD CONSOLE NORWEGIAN 95KEY	–	–	–	–	–	–	–	–	–	–	–	ALT
45														
46														
47														
48														

90

A/N: CA070057-xxx	REV. G	TITLE: ASSY KEYBOARD 1040STF(K/B)	MODEL: 1040STF (KEYBOARD)	A/N: CA070057-xxx

REV	REVISION DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		

ATARI

ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

VERSION	STANDARD	MARKET
	SEE SHEET 1.	

SHEET 3 OF 4

ITEM NO.	PART NUMBER	DESCRIPTION	QTY. REQUIRED PER VERSION -013	-014	-015	NOTE
49						
50						
51	CA070138-012	ASSY KEYBOARD CONSOLE ARABIC 95KEY	1	-	-	
52	CA070138-013	ASSY KEYBOARD CONSOLE ITALIAN 95KEY	-	1	-	
53	CA070138-014	ASSY KEYBOARD CONSOLE SWISS 95KEY	-	-	1	
54						
55						
56						
57						
58	CA200432-012	ASSY KEYBOARD CONSOLE ARABIC 95KEY	ALT	-	-	
59	CA200432-013	ASSY KEYBOARD CONSOLE ITALIAN 95KEY	-	ALT	-	
60	CA200432-014	ASSY KEYBOARD CONSOLE SWISS 95KEY	-	-	ALT	
61						
62	—					
63						
64						
65	C103418-013	KEYBOARD 95KEY ARABIC	ALT	-	-	
66	C103496-013	KEYBOARD 95KEY ITALIAN	-	ALT	-	
67						
68						
69						
70						
71						
72						
73						
74						
75	C070122-002	IC 6301V1 1CHIP CPU VER 63V 2.0	1	1	1	
76						
77						
78						
79						
80						
81						
82						
83						
84						
85						
86						
87						
88						
89						
90						
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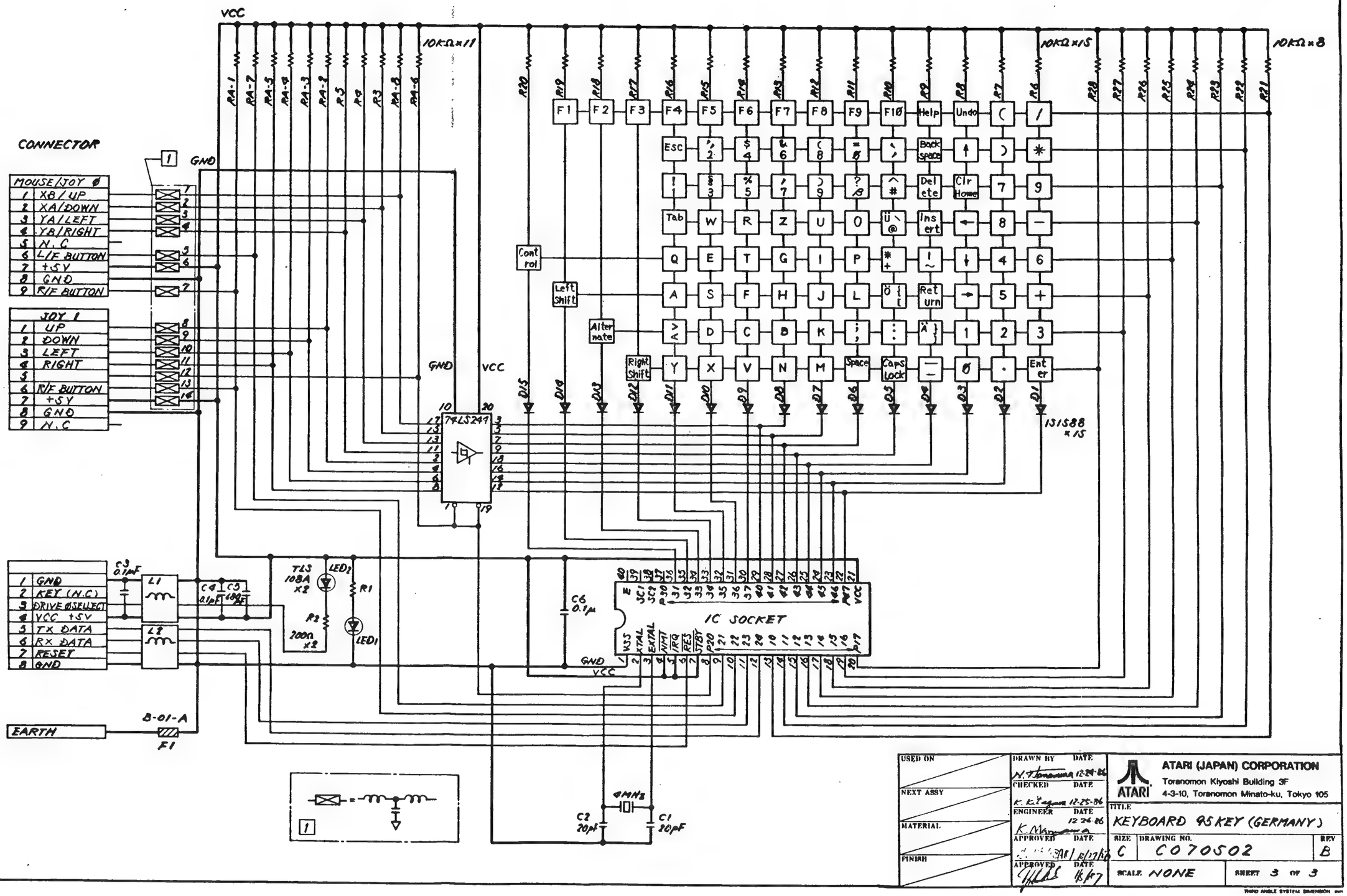
92						
93						
94						
95						
96						

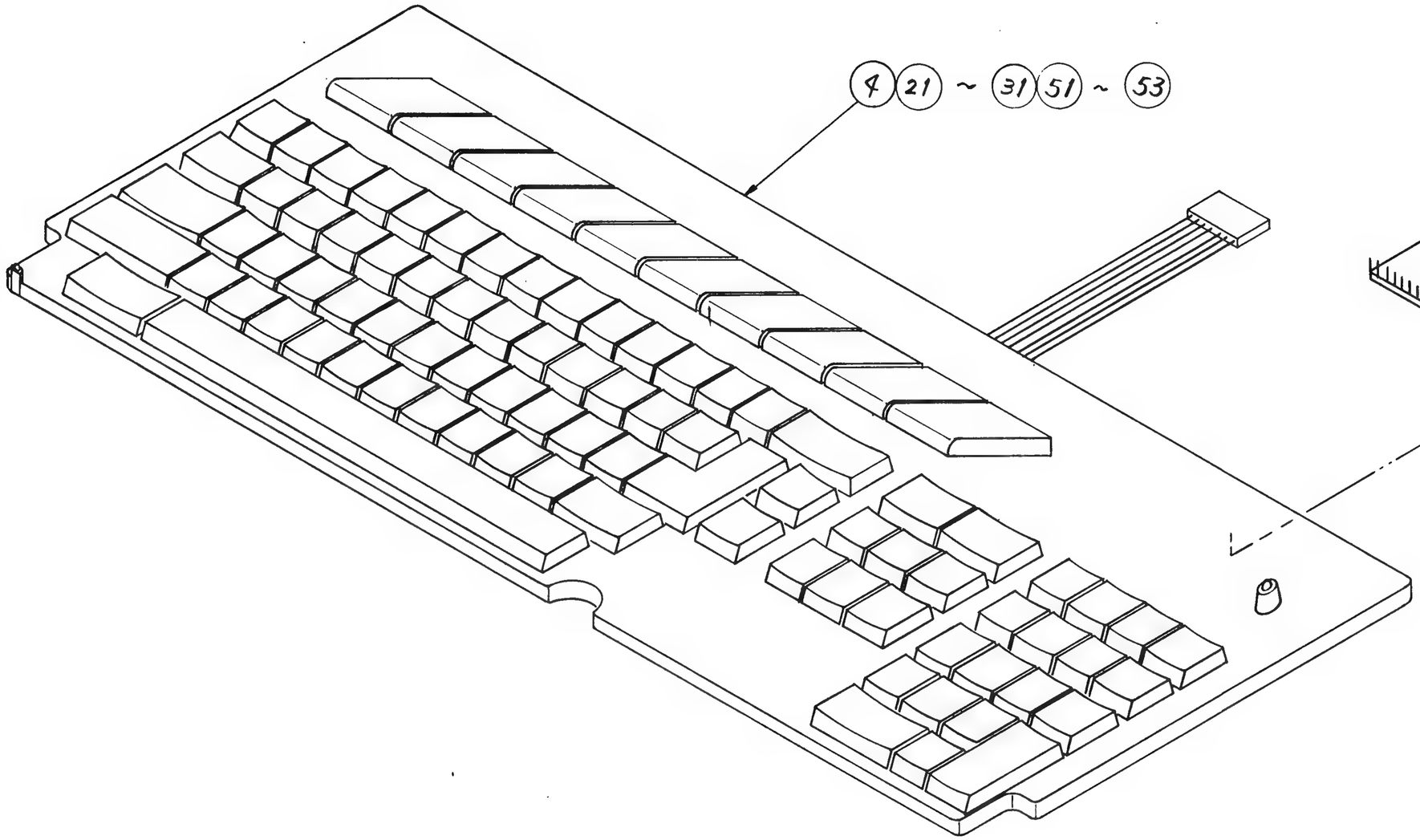
REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON	DRAWN BY N. Tonomura	DATE 12-24-86	ATARI (JAPAN) CORPORATION Toranomon Kiyoshi Building 3F 4-3-10, Toranomon Minato-ku, Tokyo 105
NEXT ASSY	CHECKED K. Kitagawa	DATE 12-25-86	
MATERIAL	ENGINEER K. Mano	DATE 12-26-86	TITLE KEYBOARD 95KEY (GERMANY)
FINISH	APPROVED	DATE 12/27/86	SIZE C · DRAWING NO. C070502 · REV B
	APPROVED	DATE 1/6/87	SCALE NONE · SHEET 3 OF 3

THIRD ANGLE SYSTEM DIMENSION mm

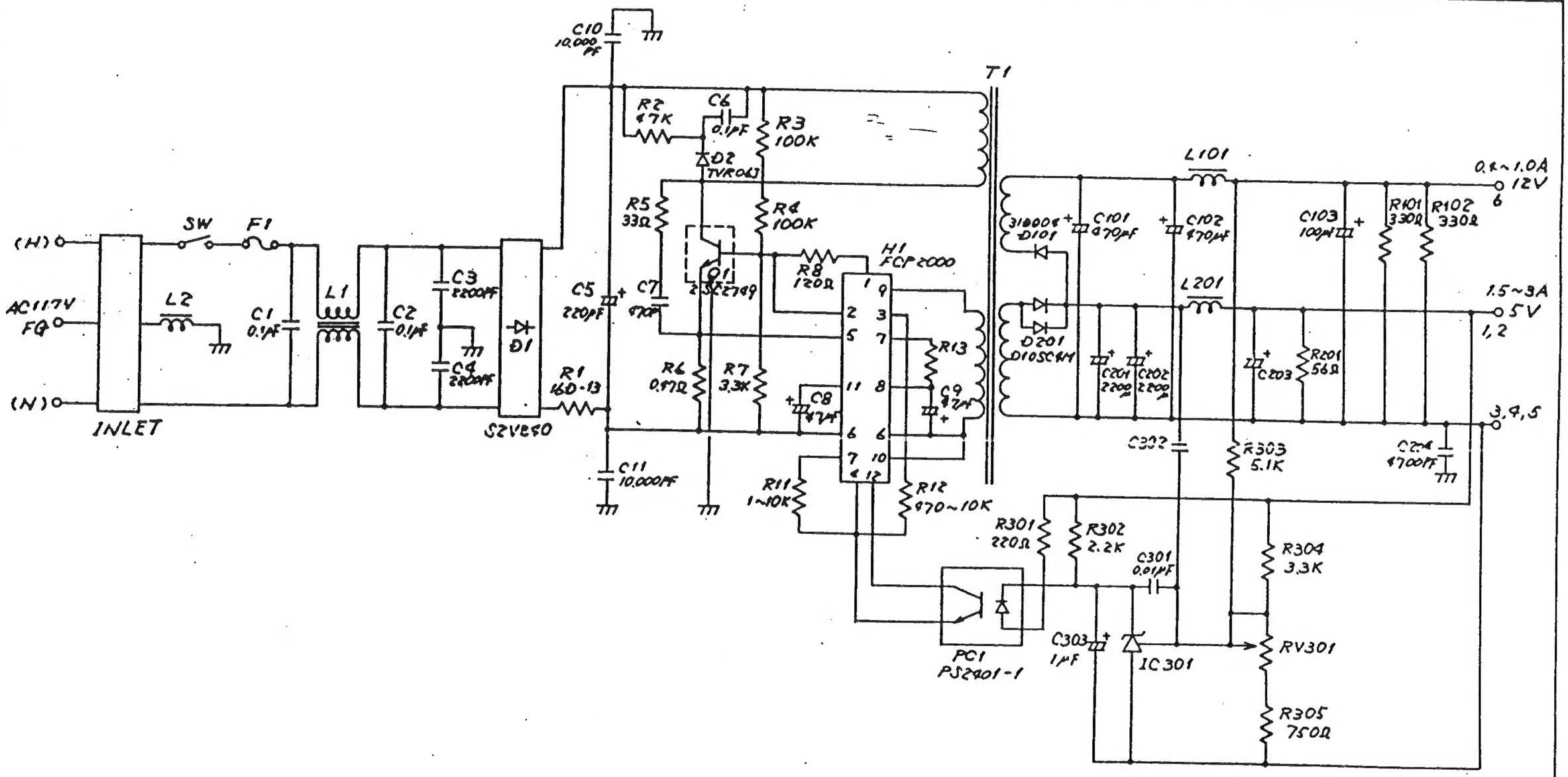
REV	REVISIONS DESCRIPTION	DATE	APPROVED
	SEE SHEET 1.		



USED ON	DRAWN BY N. Hanamura 9-19-85	ATARI (JAPAN) CORPORATION Toranomon Kiyoshi Building 3F 4-3-10, Toranomon Minato-ku, Tokyo 105
NEXT ASSY	CHECKED K. Kitagawa 10-11-85	TITLE: ASSY KEYBOARD 1040STF (K/B)
MATERIAL	ENGINEER Sm. 10.11.85	SIZE B; DRAWING NO. CA070057-XXX; REV G
FINISH	APPROVED 7/12/88	SCALE NONE; SHEET 4 OF 4
	APPROVED 10/12/85	THIRD ANGLE SYSTEM DIMENSION mm

Power Supply

REV	REVISIONS DESCRIPTION	DATE	APPROVED



TOLERANCES	
UNDER 30	±0.1
30 THRU 300	±0.2
OVER 300	±0.4

USED ON

NEXT ASSY

MATERIAL

FINISH

DRAWN BY I. Yoshida DATE 4/30/86

CHECKED DATE

ENGINEER DATE

APPROVED DATE

APPROVED DATE

ATARI

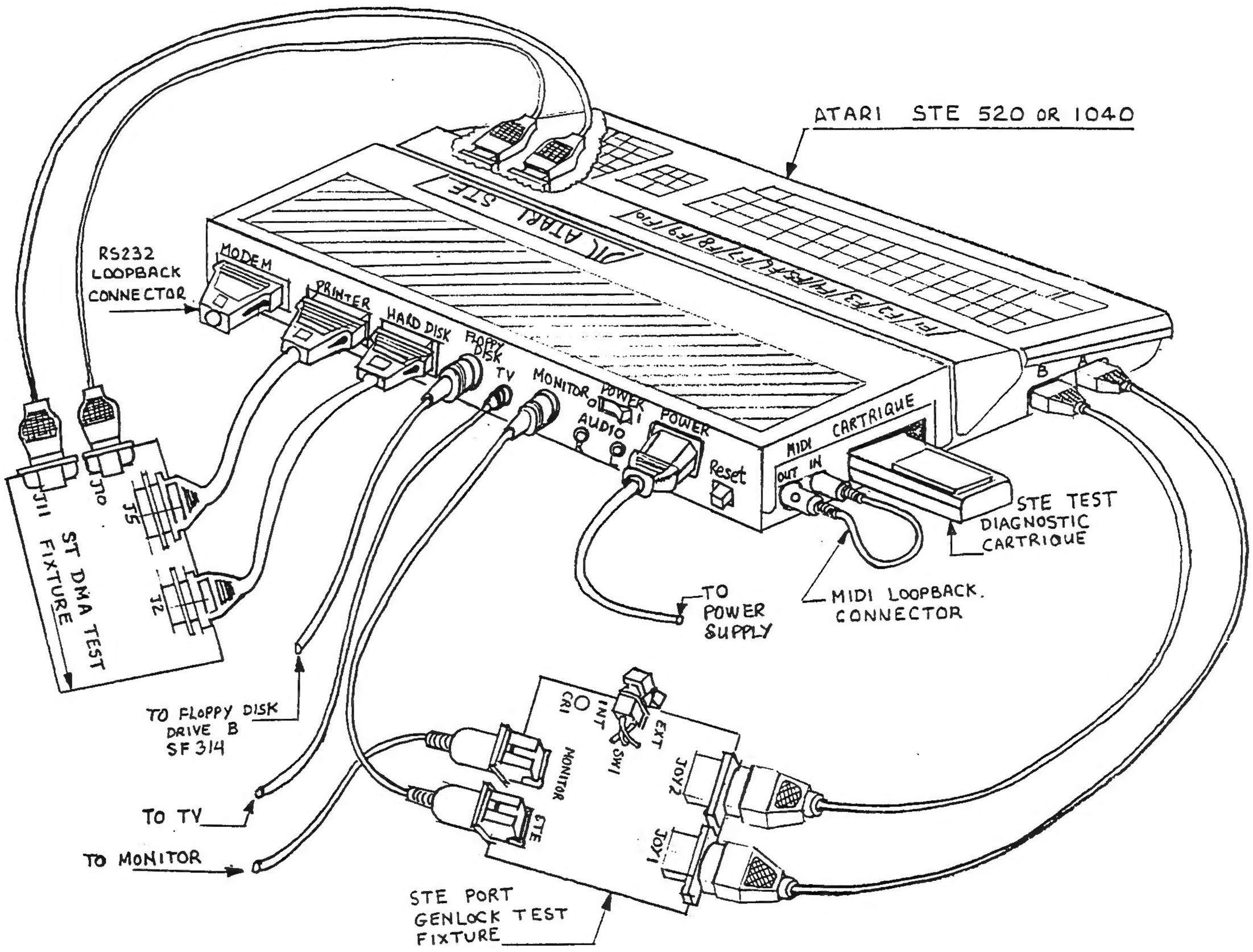
ATARI (JAPAN) CORPORATION
Toranomon Kiyoshi Building 3F
4-3-10, Toranomon Minato-ku, Tokyo 105

TITLE
TYPICAL 1040STF(M) POWER SUPPLY

SIZE B DRAWING NO. REV

SCALE NONE SHEET 1 OF 1

STE Test Fixture


ATARI STE 520 OR 1040
RS232
LOOPBACK
CONNECTOR
MODEM
PRINTER
HARD DISK
FLOPPY DISK
TV
MONITOR
AUDIO
POWER
POWER
Reset
MIDI
CARTRIQUE
OUT IN
STE TEST
DIAGNOSTIC
CARTRIQUE
TO
POWER
SUPPLY
MIDI LOOPBACK.
CONNECTOR
J11
J10
J5
J2
ST DMA TEST
FIXTURE
TO FLOPPY DISK
DRIVE B
SF 314
TO TV
TO MONITOR
INT
CR1
EXT
SW1
MONITOR
STE
JOY2
JOY1
STE PORT
GENLOCK TEST
FIXTURE